Elzar

Triple Modular Redundancy using Intel AVX

Dmitrii Kuvaiskii

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Hardware Errors in the Wild

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„…There were a handful of messages that had **a single bit corrupted** such that the message was **still intelligible**, but the system state information was **incorrect**…“

Mesa: Geo-Replicated, Near Real-Time, Scalable Data Warehousing

Ashish Gupta, Fan Yang, Jason Govig, Adam Kirsch, Kelvin Chan
Kevin Lai, Shuo Wu, Sandeep Govind Dhoot, Abhilash Rajesh Kumar, Ankur Agiwal
Sanjay Bhansali, Mingsheng Hong, Jamie Cameron, Masood Siddiqi, David Jones
Jeff Shute, Andrey Gubarev, Shivakumar Venkataraman, Divyakant Agrawal
Google, Inc.

„…Corruption can occur **transiently in CPU** or RAM. Guarding against such corruptions is an **important goal** in Mesa’s overall design…“

Protecting Against Data Corruptions

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Byzantine Fault Tolerance

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☺ Tolerates arbitrary faults

☹ Pessimistic fault model

☹ High resource overheads

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Checksums / Assertions

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- ☺ Tolerates arbitrary faults
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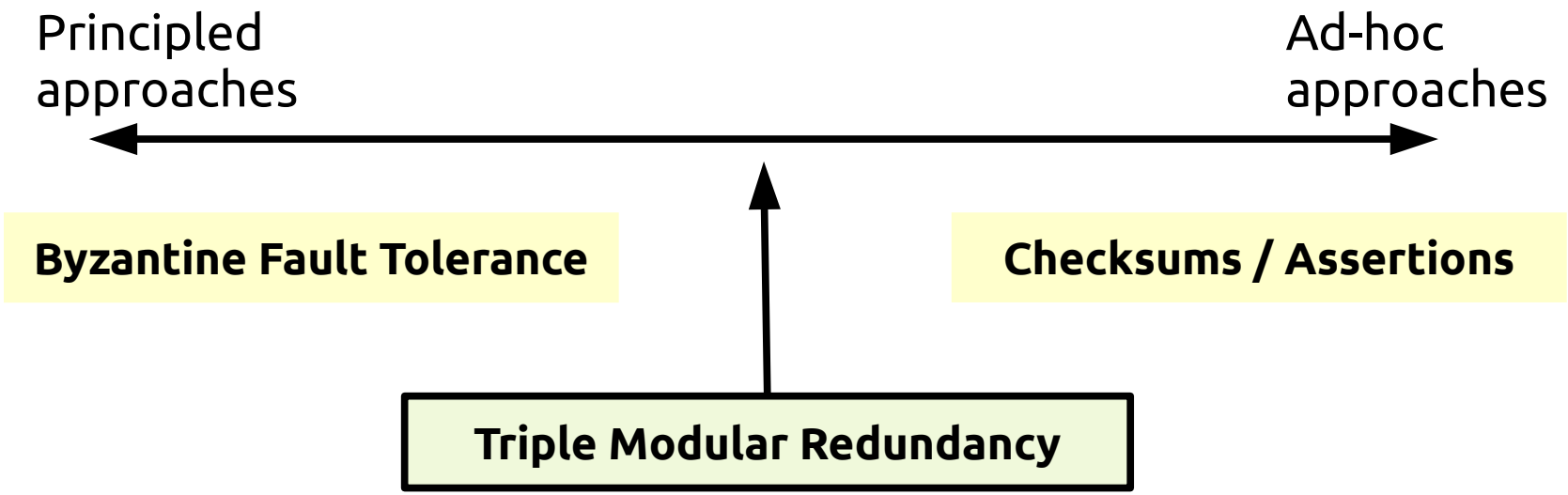
- ☹ High resource overheads

Checksums / Assertions

- ☺ Low performance overheads
- ☹ Only anticipated faults
- ☹ Manual and error-prone

Protecting Against Data Corruptions



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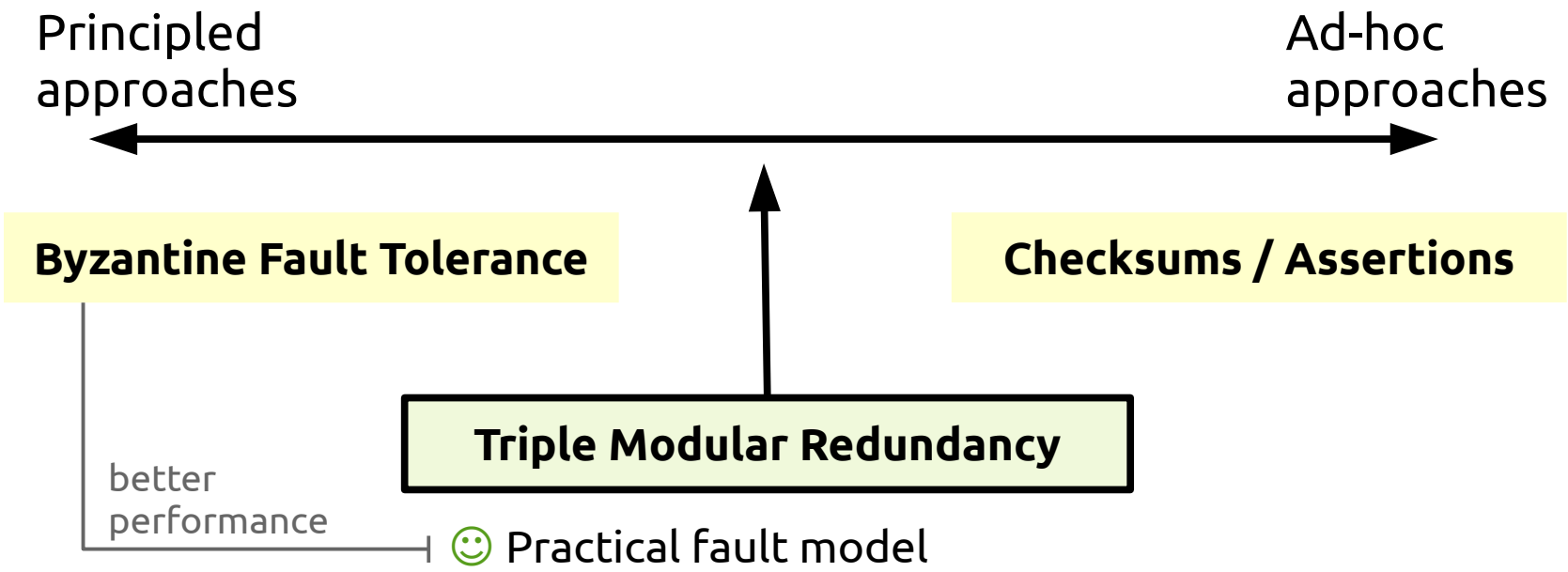

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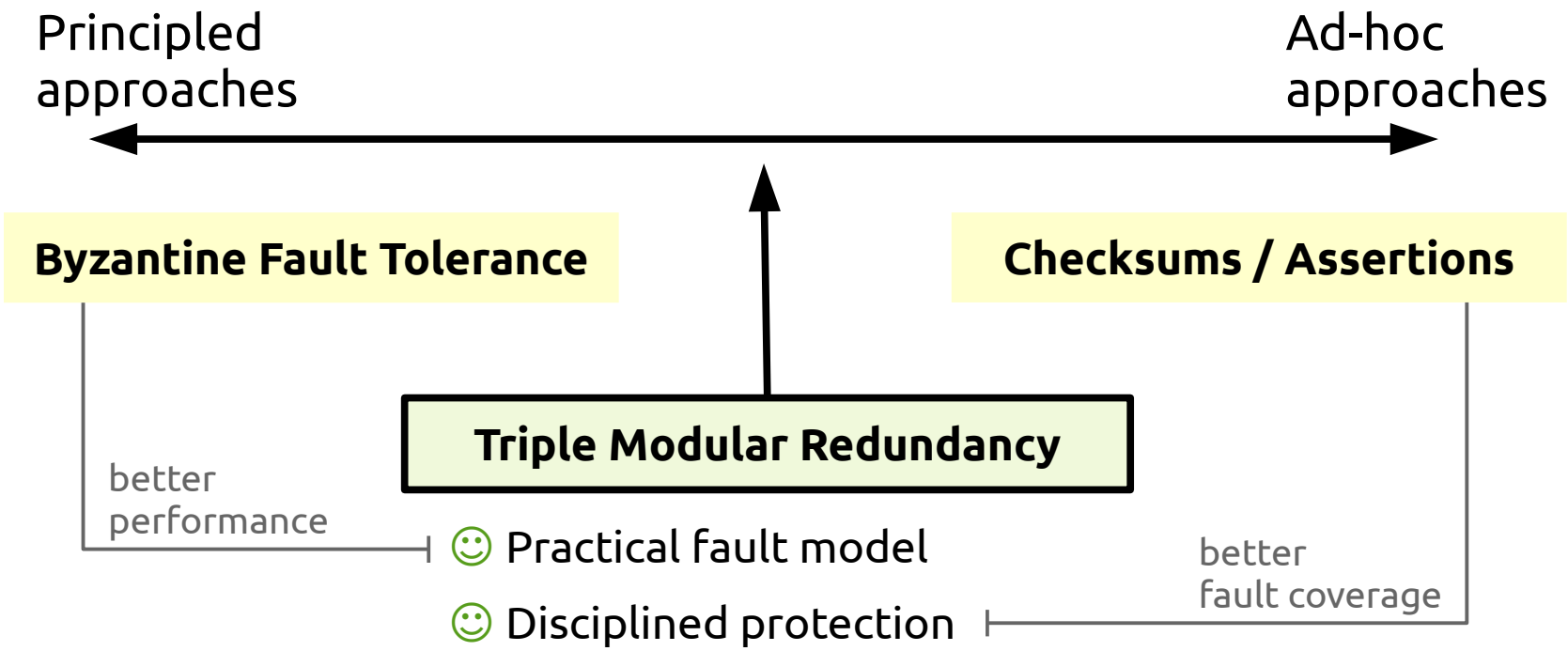
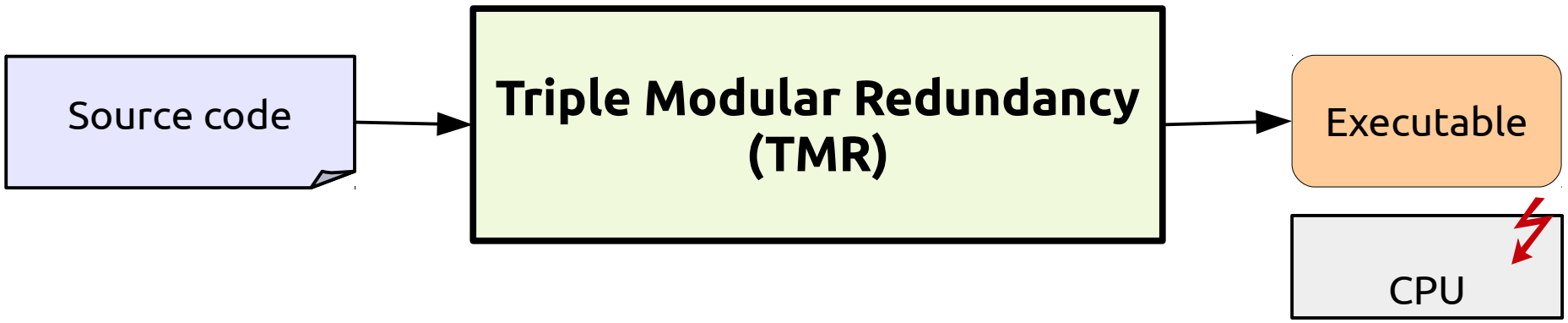


Triple Modular Redundancy



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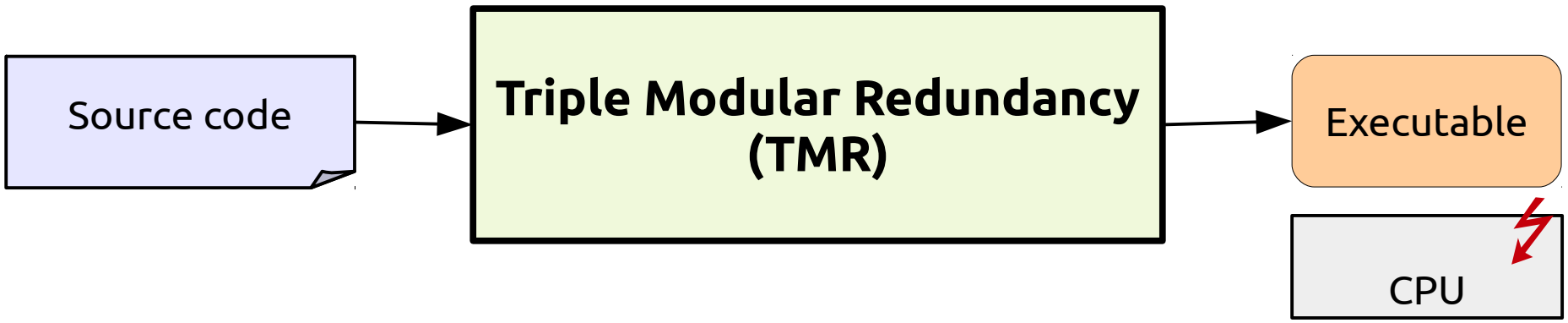

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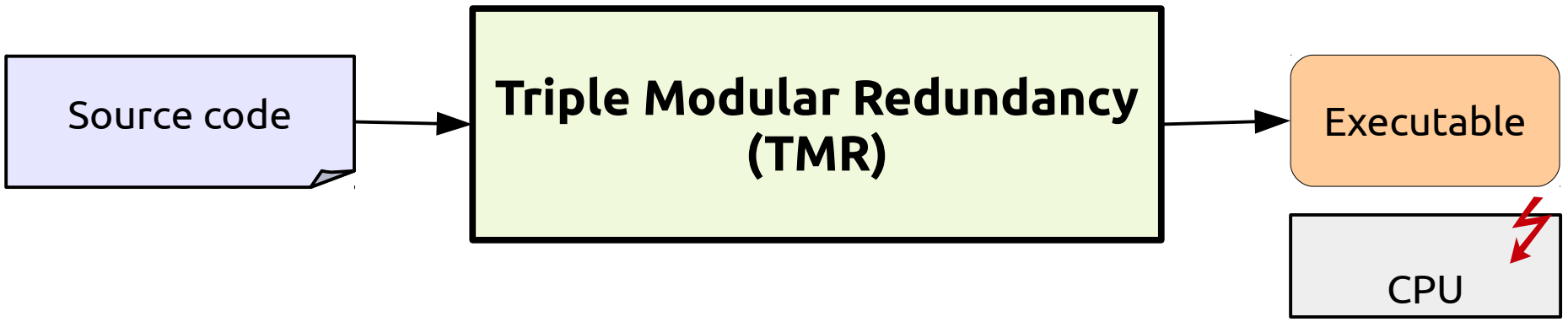

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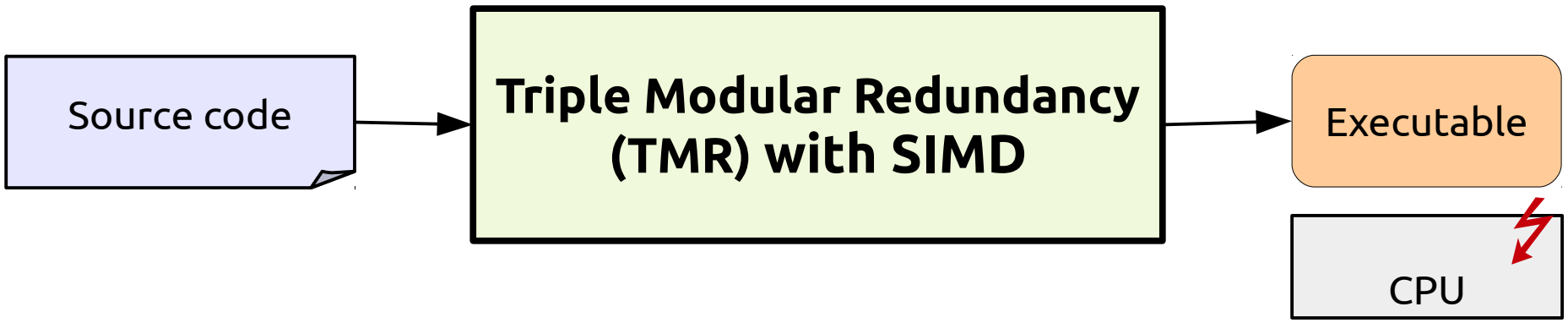

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TMR with SIMD

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zwide = add xwide, ywide
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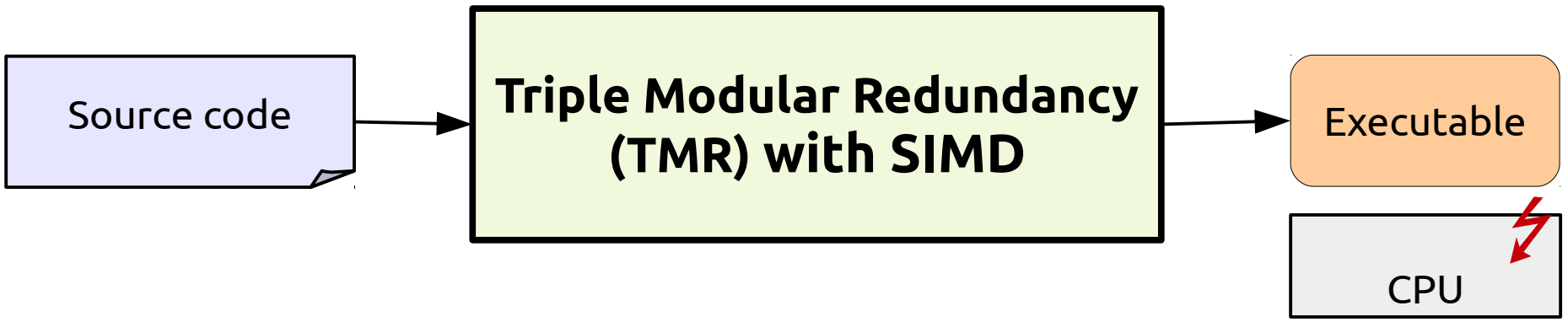

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TMR with SIMD

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zwide = add xwide, ywide
```

Idea **SIMD** uses less instructions → **less perf overhead?**

Research Question

Can we use **SIMD** for **efficient fault tolerance**?

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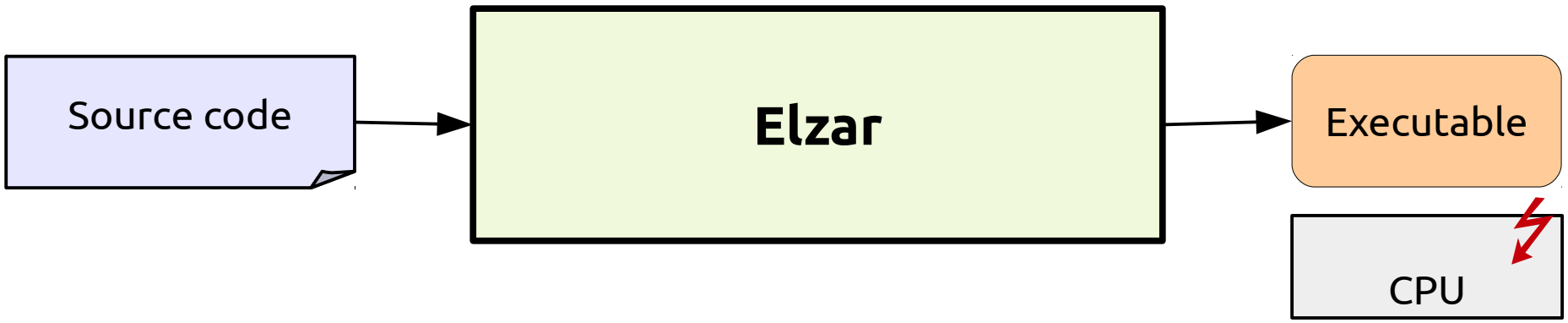
Implementation using **Intel AVX**

Elzar



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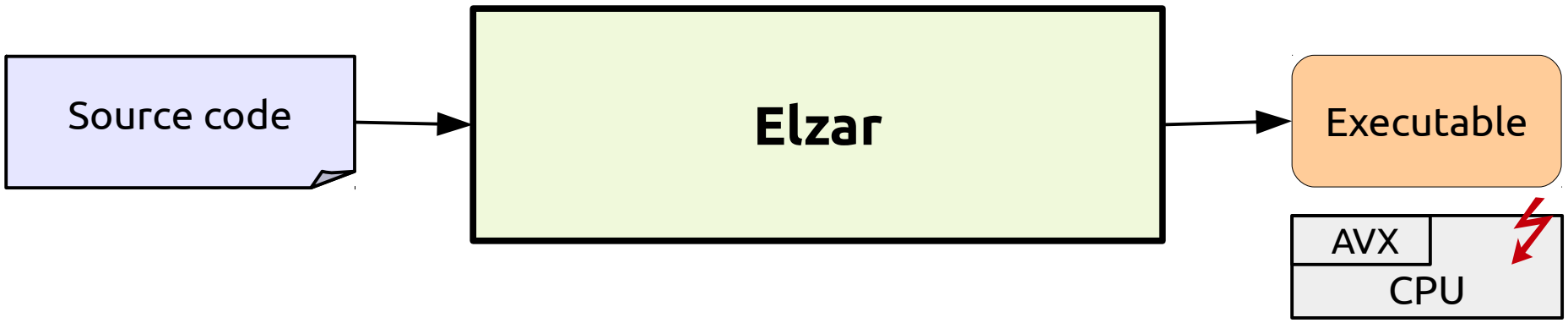
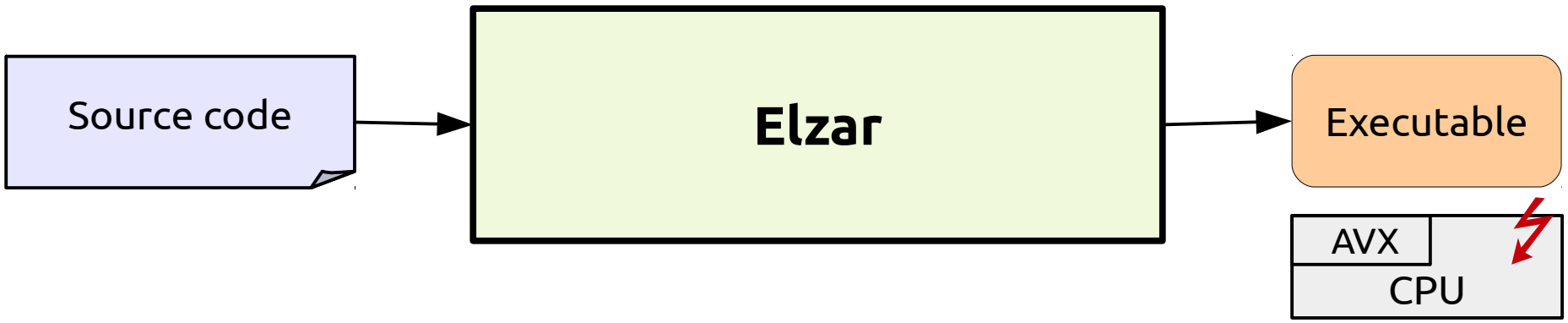


Implementation **Intel AVX** for triple modular redundancy

Elzar



Implementation **Intel AVX** for triple modular redundancy

Outcome **Mixed results** ☹ (AVX not general-purpose)

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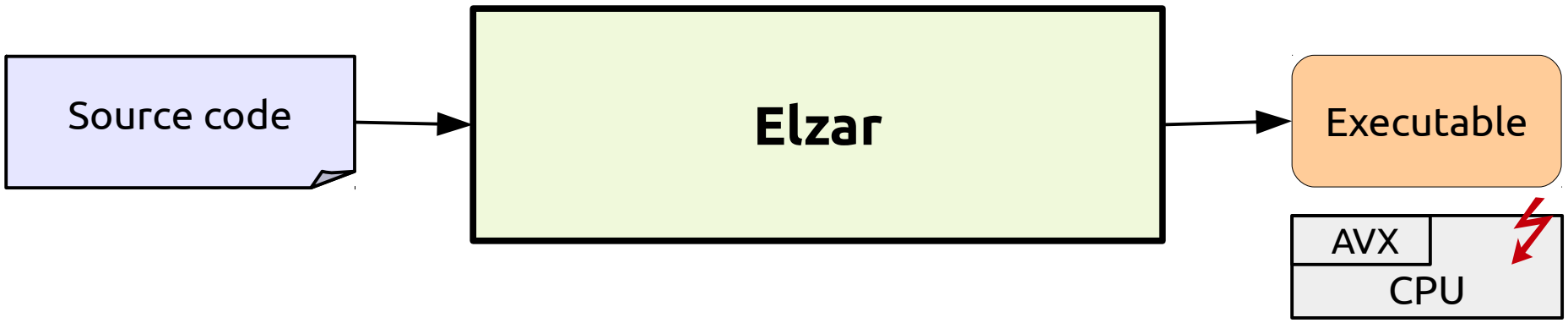

Implementation **Intel AVX** for triple modular redundancy

Outcome **Mixed results** ☹ (AVX not general-purpose)

Investigation **Two bottlenecks** in current AVX

☑ Motivation

☐ **Intel AVX**

☐ Design

☐ Evaluation

☐ Discussion

Intel AVX Background

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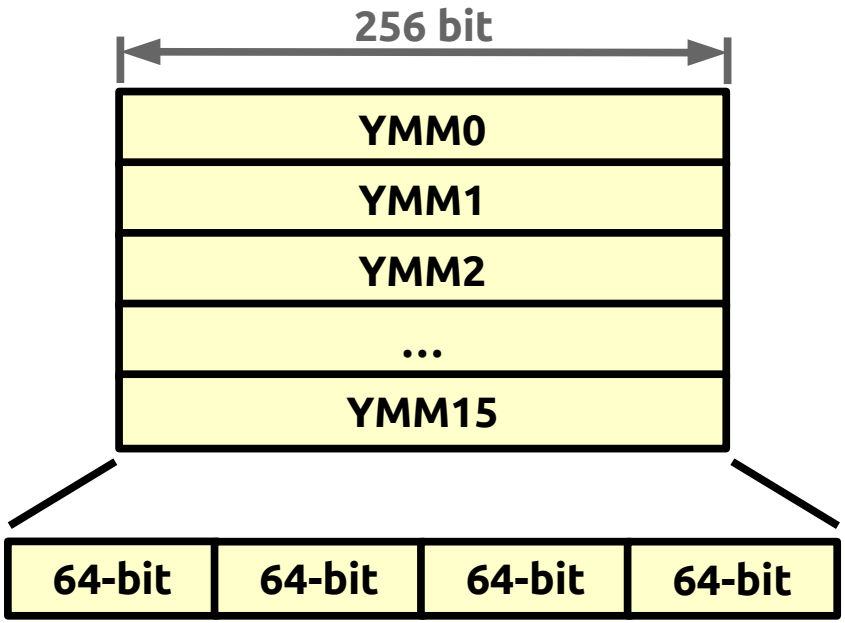
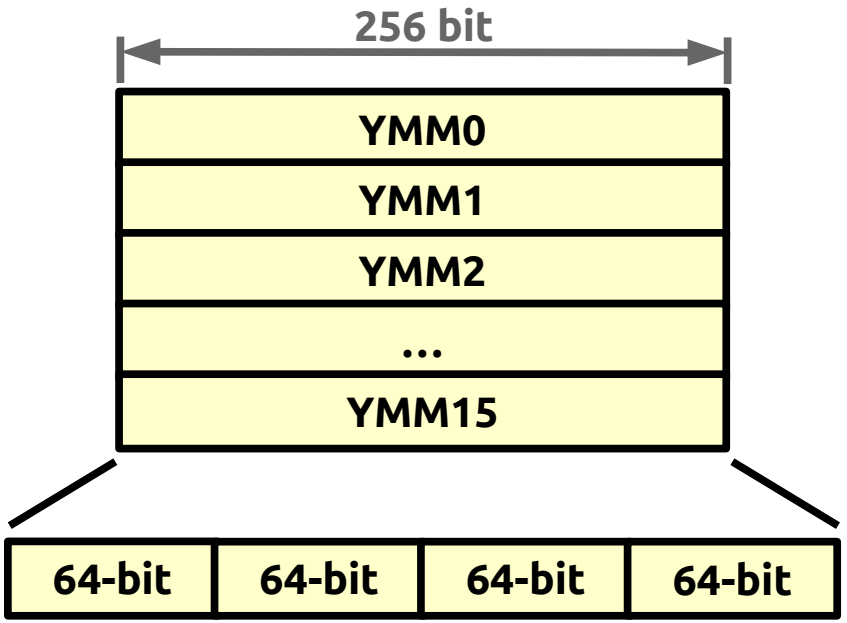
New registers

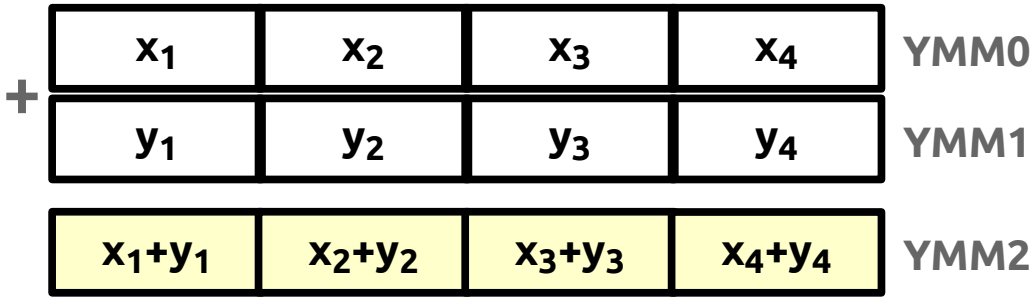


Intel AVX Background

New registers



New instructions



AVX as free resource?

AVX is not actively used?

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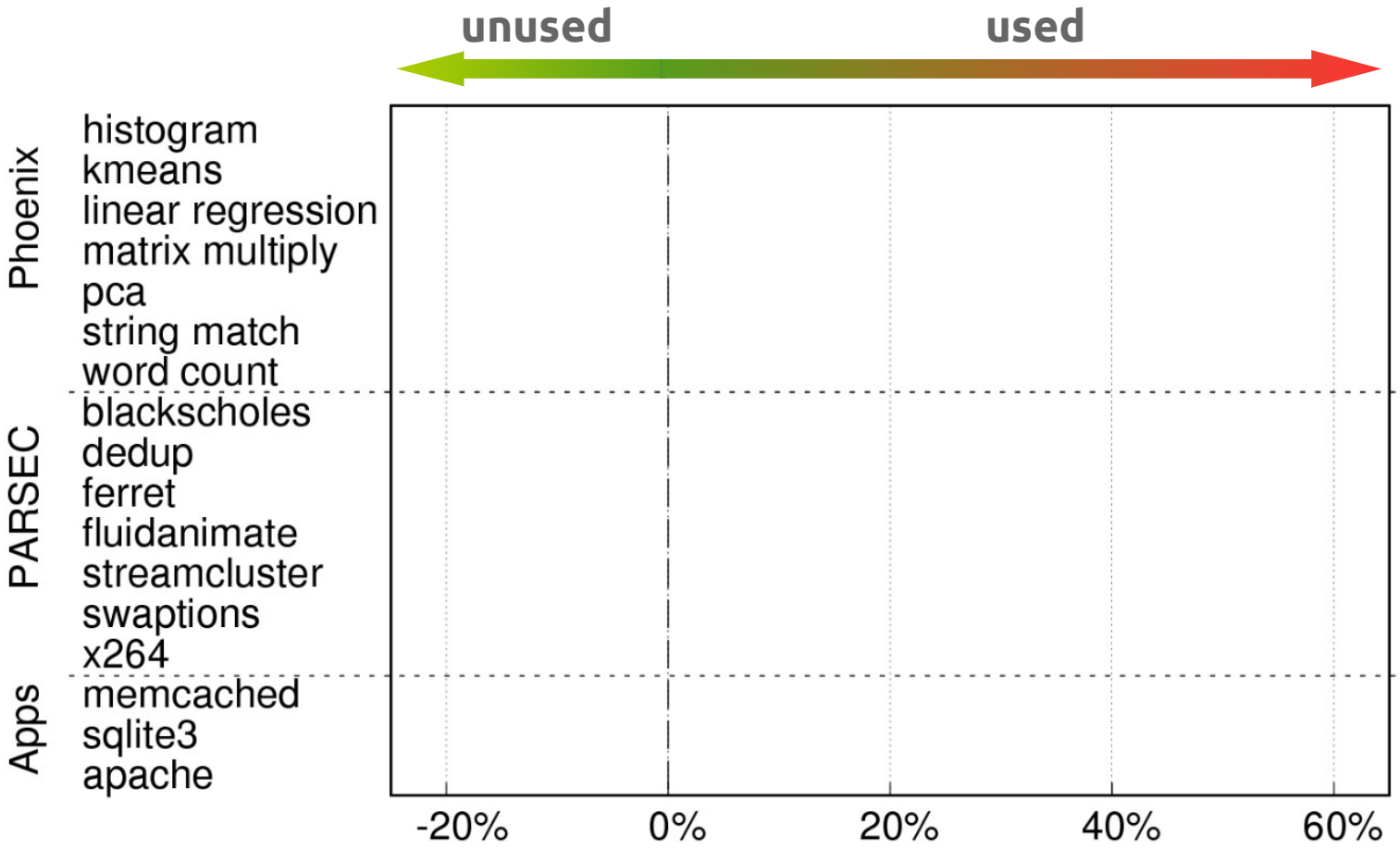

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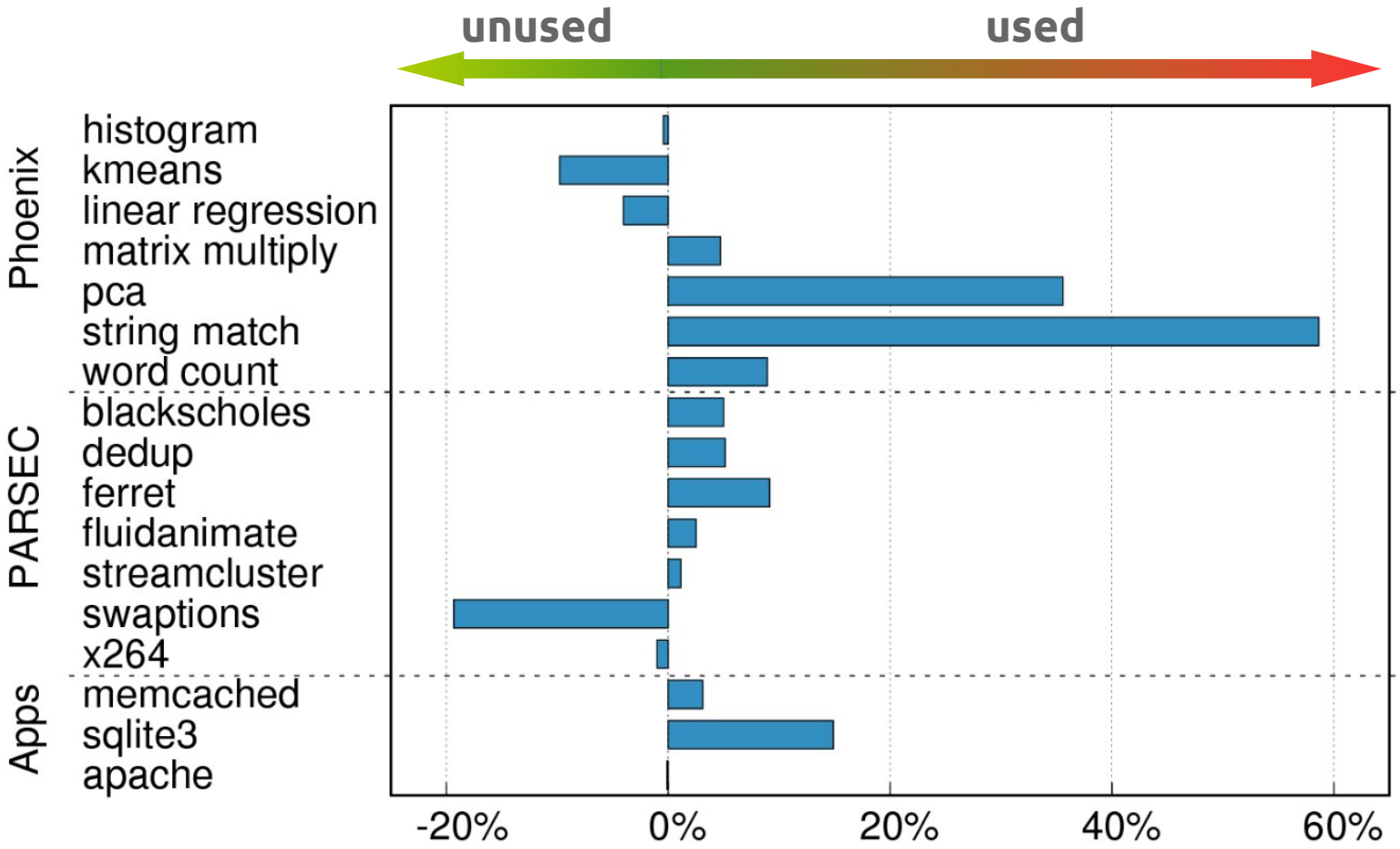

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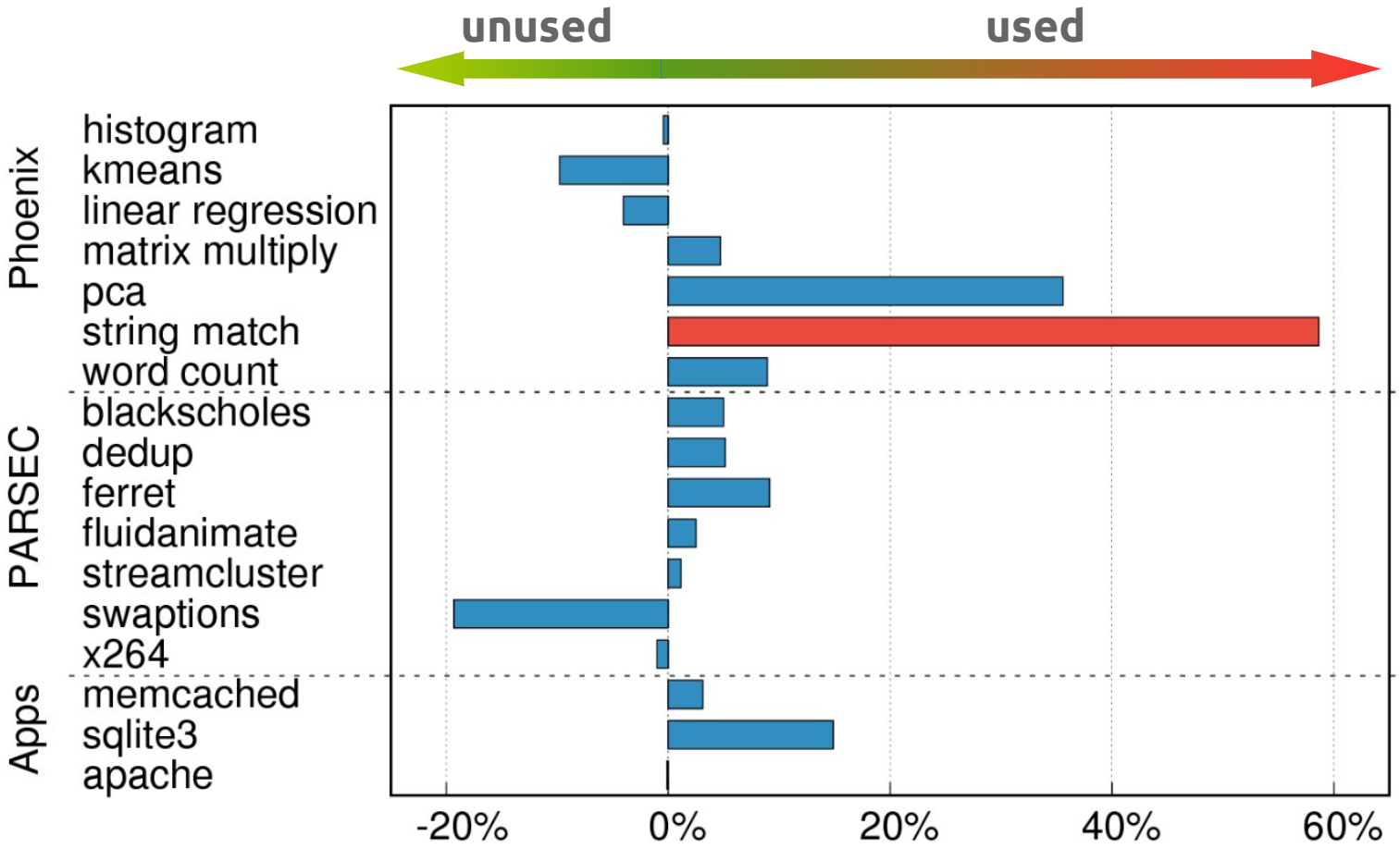
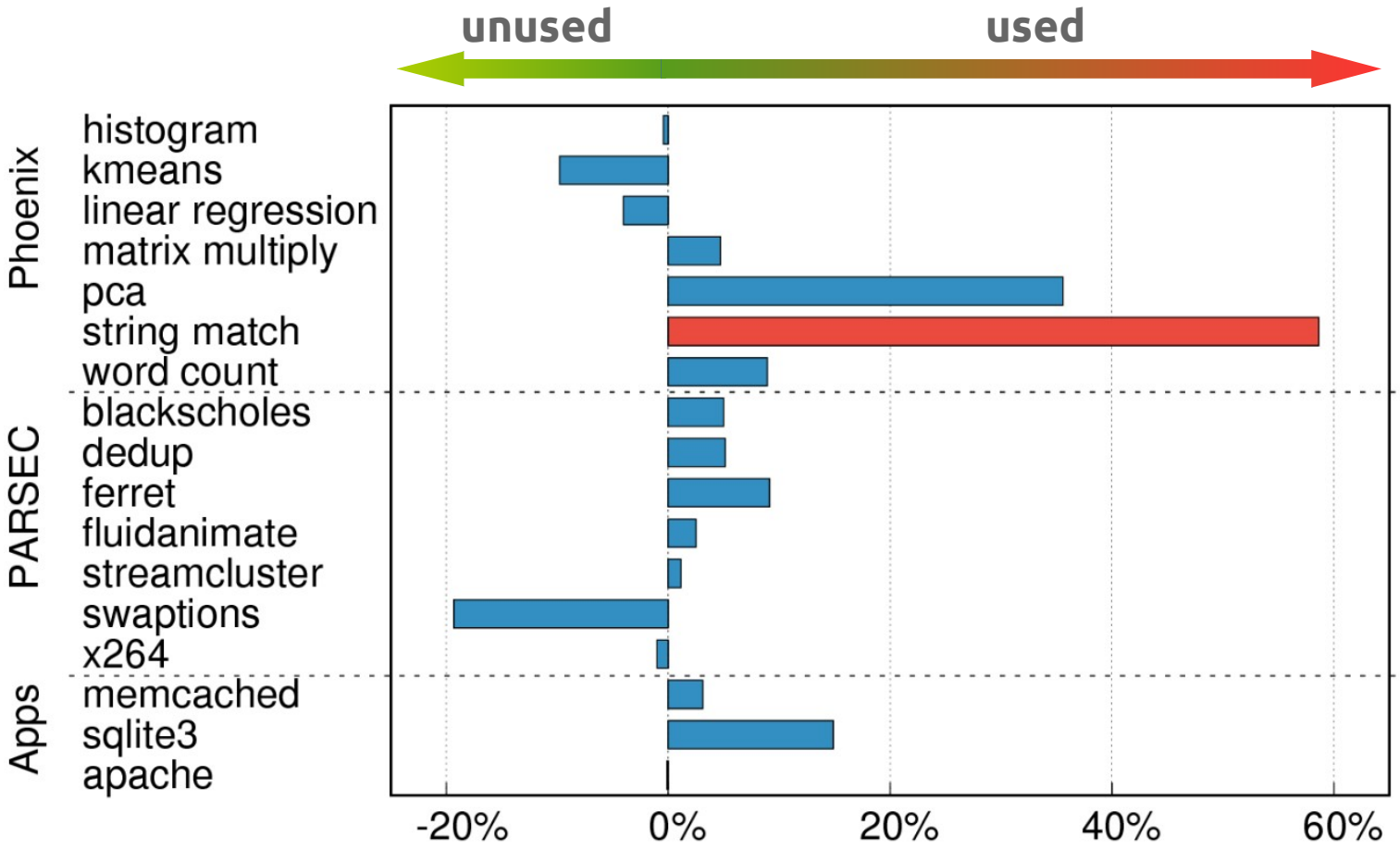


AVX as free resource?

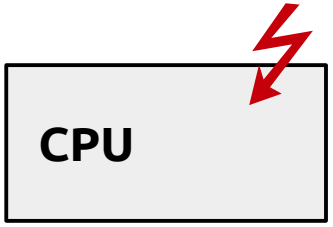
AVX is not actively used? → **Reuse for fault tolerance!**



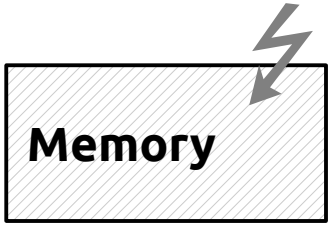
- ☑ Motivation
- ☑ Intel AVX
- ☐ **Design**
- ☐ Evaluation
- ☐ Discussion

Fault Model

- Protect against **transient faults in CPU**
  - corruptions in CPU registers
  - miscomputations in CPU execution units



- Memory is **protected by other means**
  - DRAM protected by ECC
  - CPU caches protected by ECC and parity



Elzar by Example

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Common instructions introduce lower overhead ☺

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Bottleneck 1: Memory accesses require wrappers ☹

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Bottleneck 2: Checks are expensive ☹

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No such thing as avx-load! ☹

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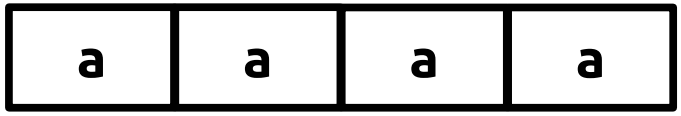

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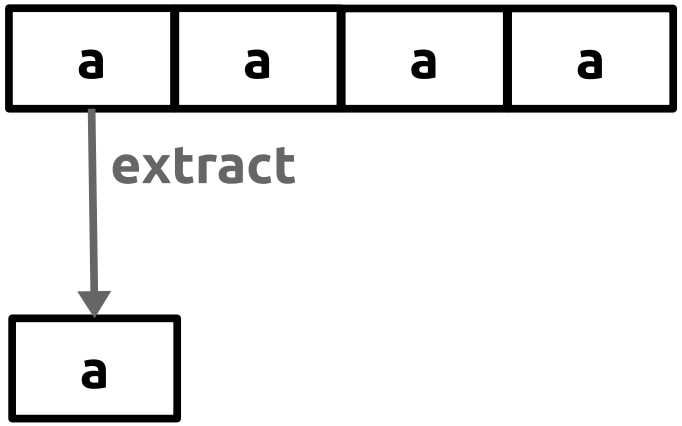

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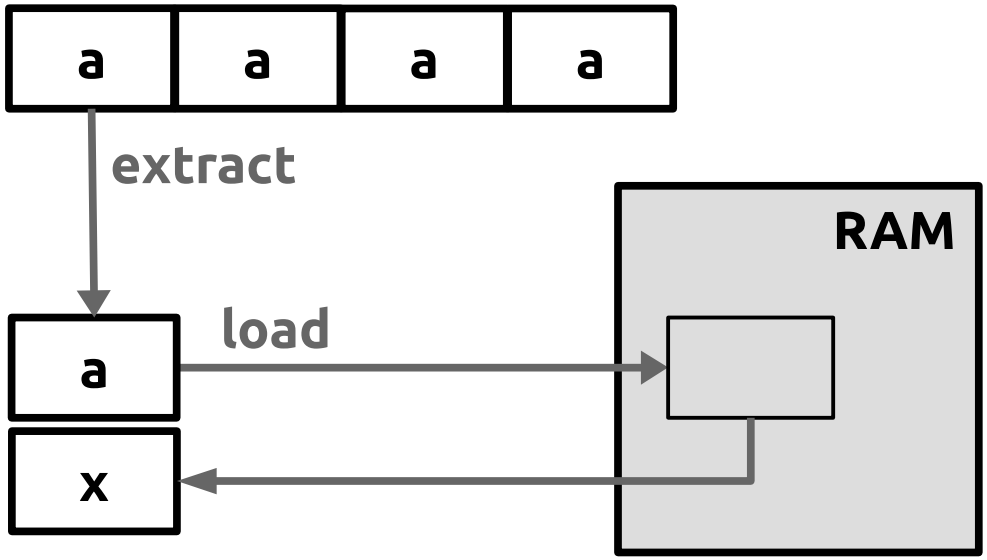

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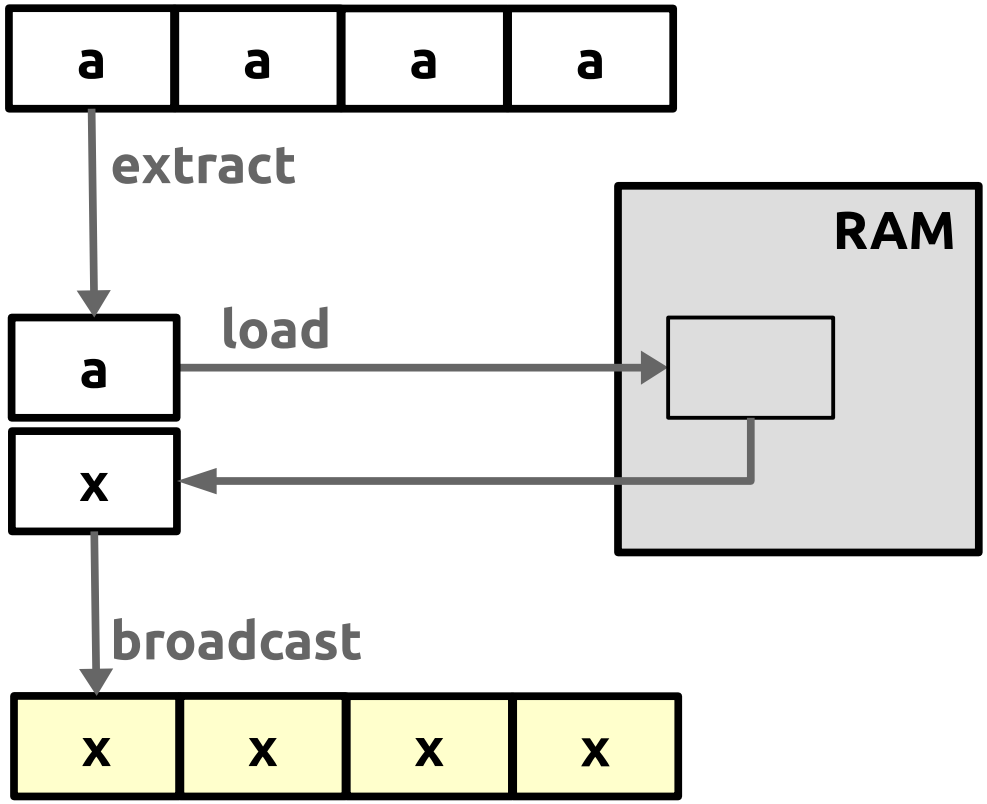

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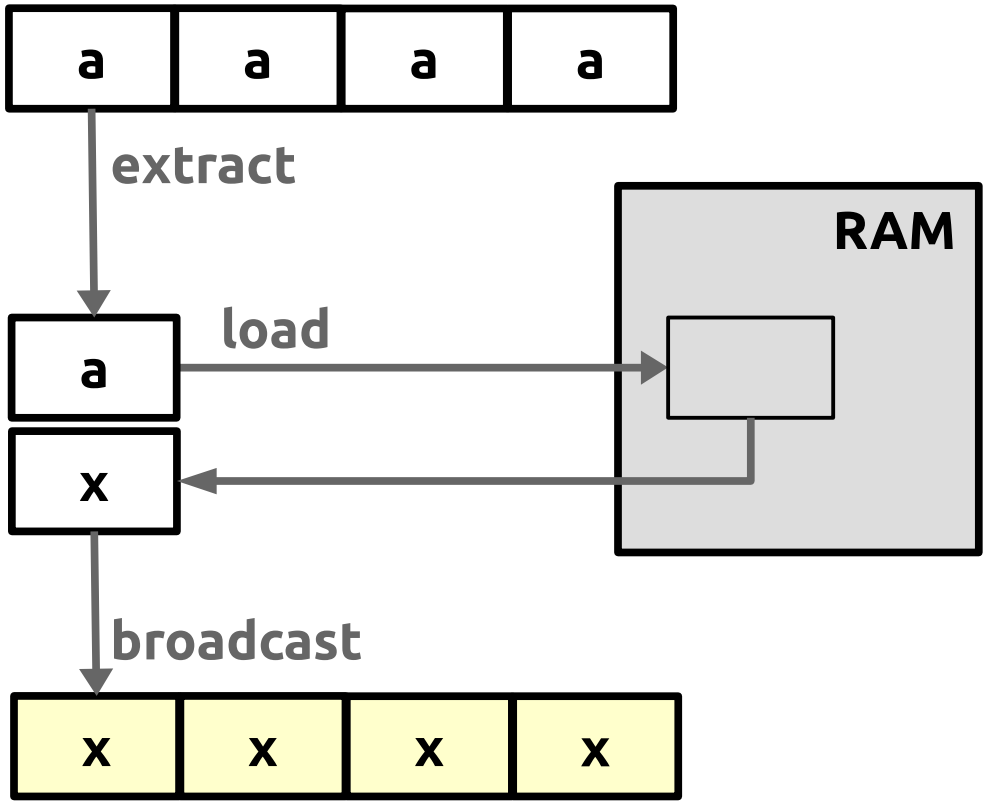

Memory accesses require wrappers ☹

Bottleneck 2: Checks

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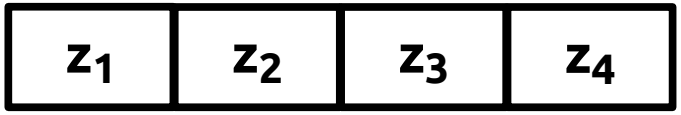

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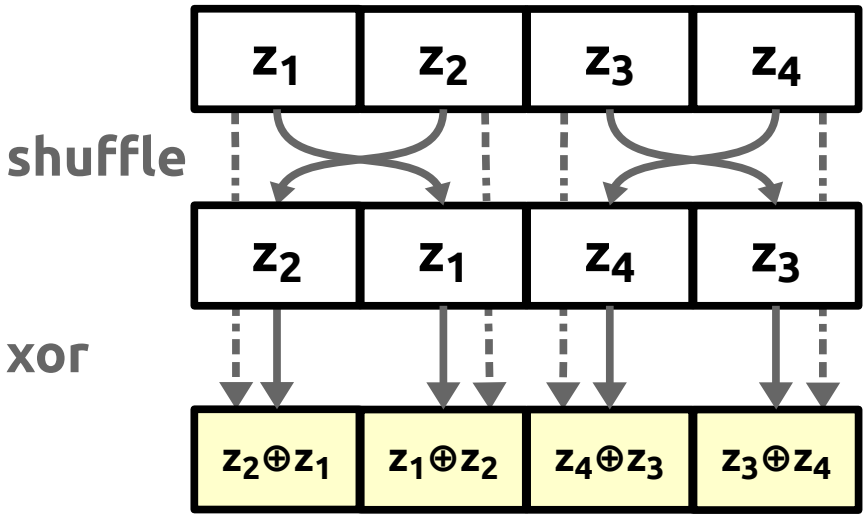

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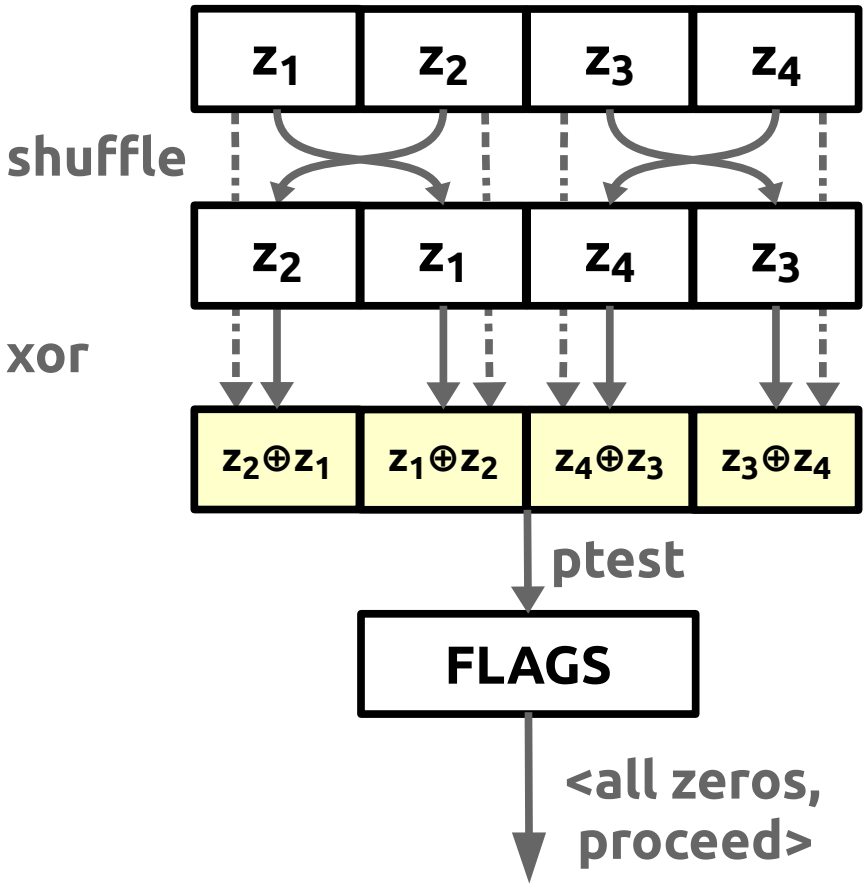

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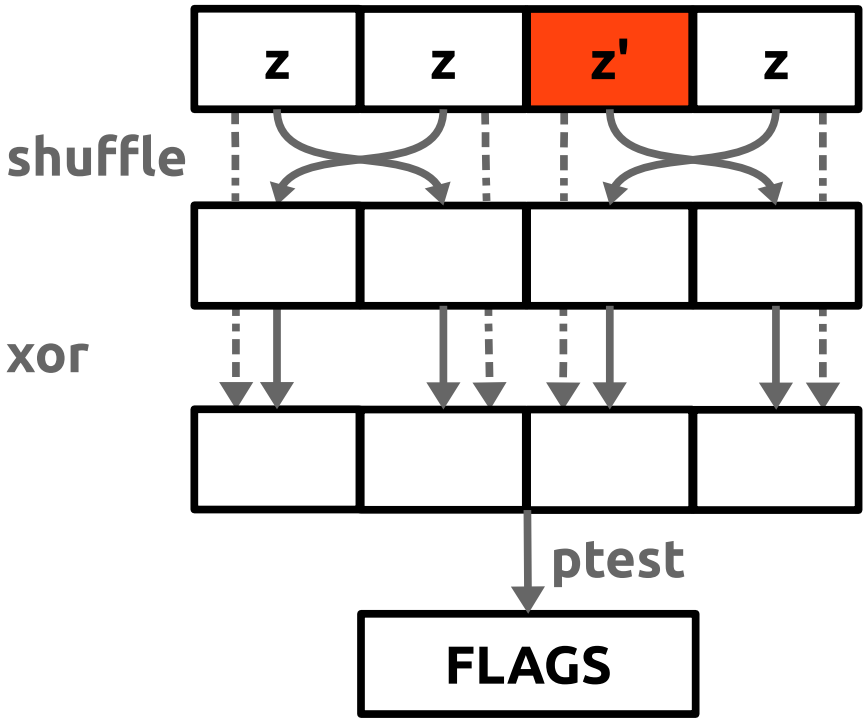

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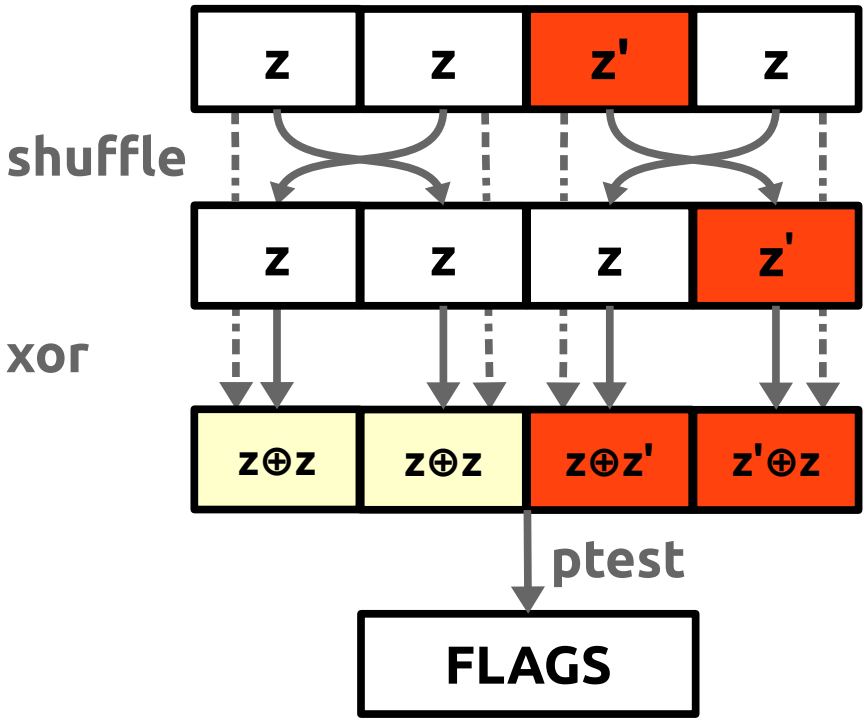

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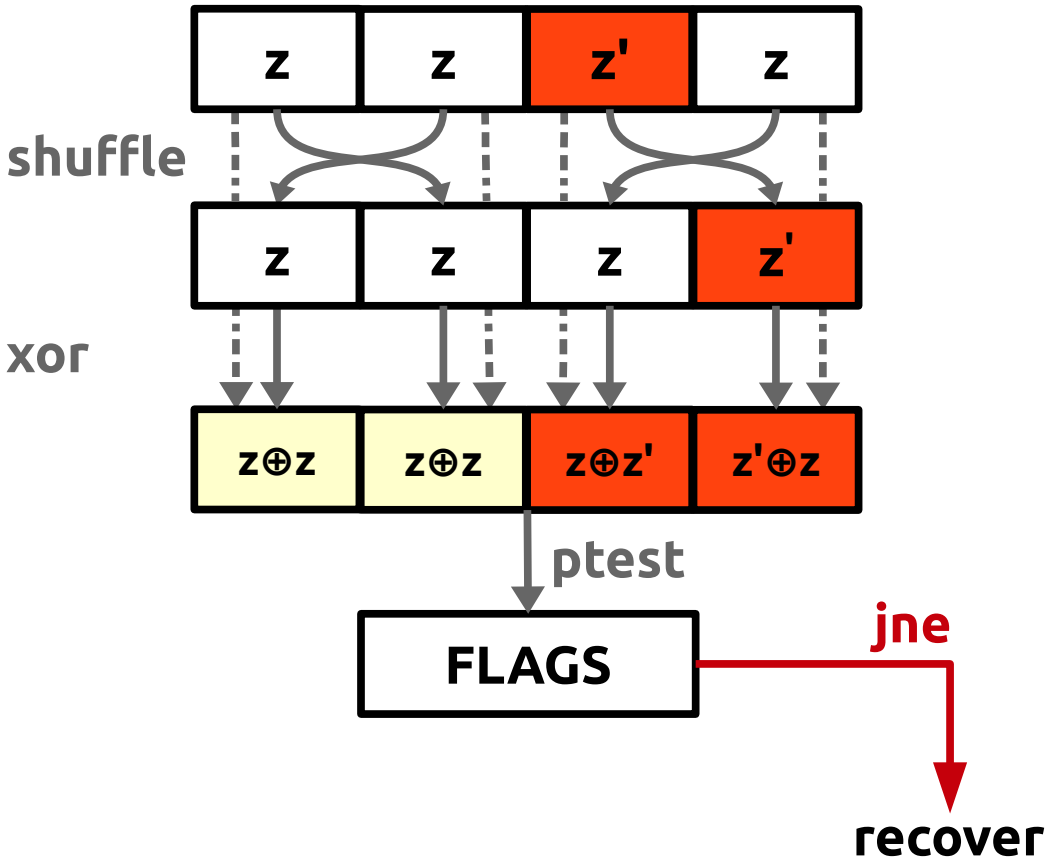

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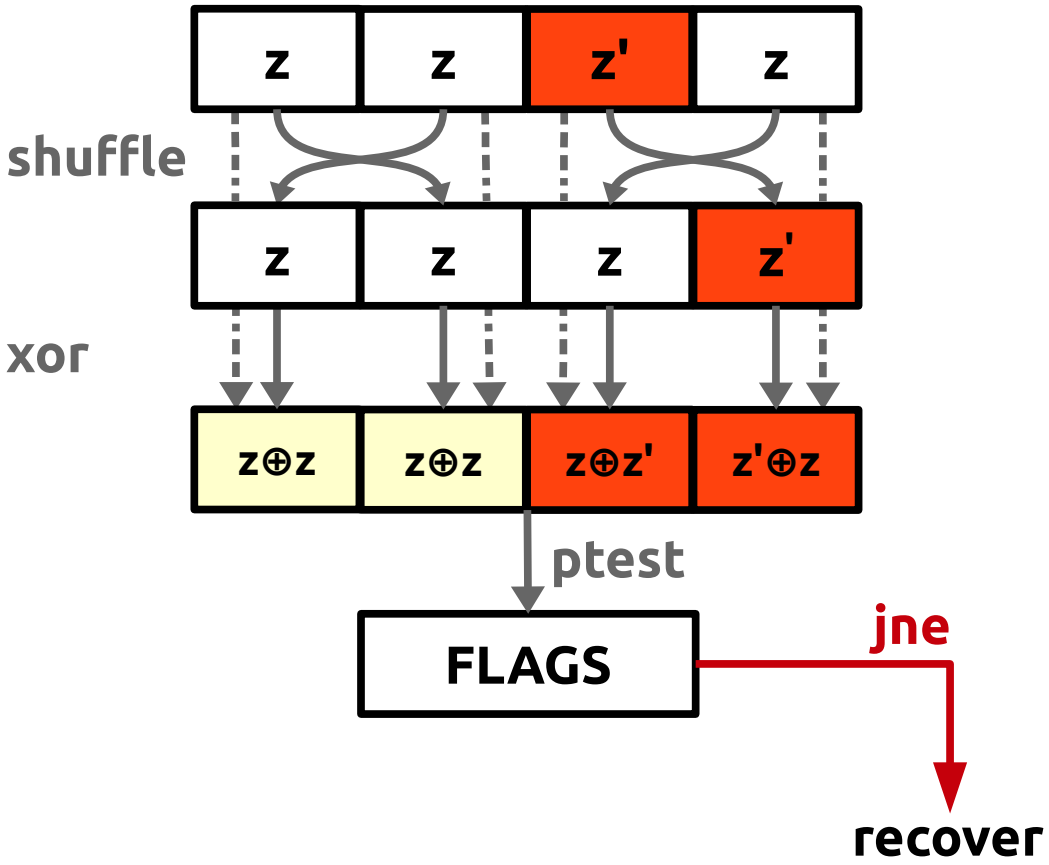
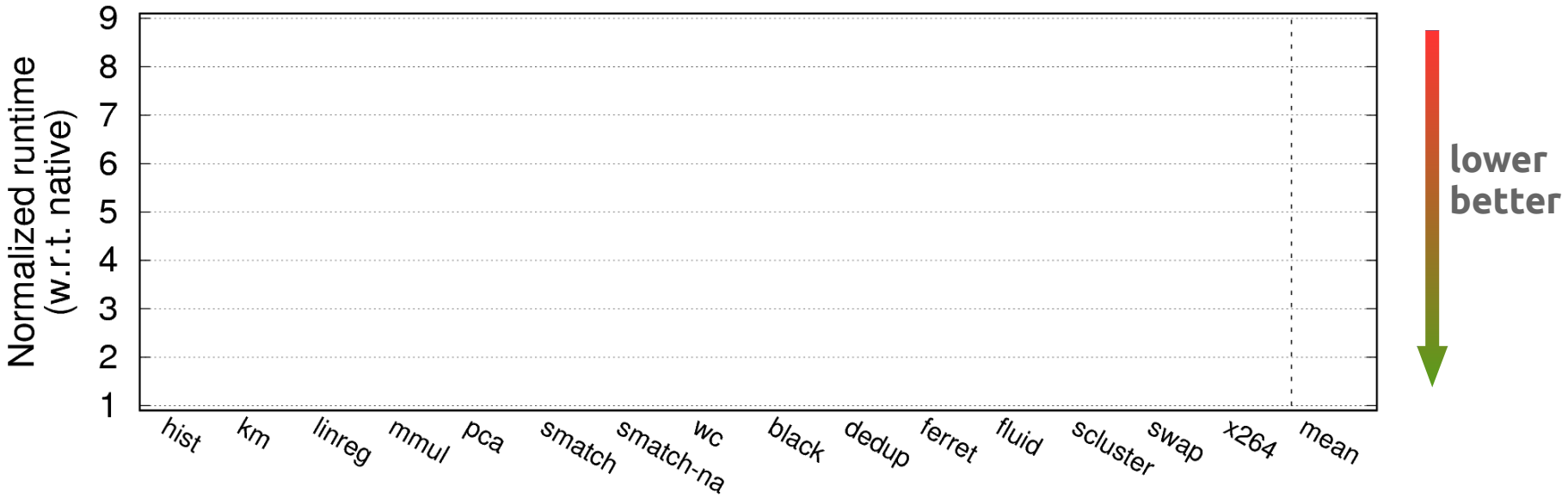


Checks introduce additional **55%** overhead ☹

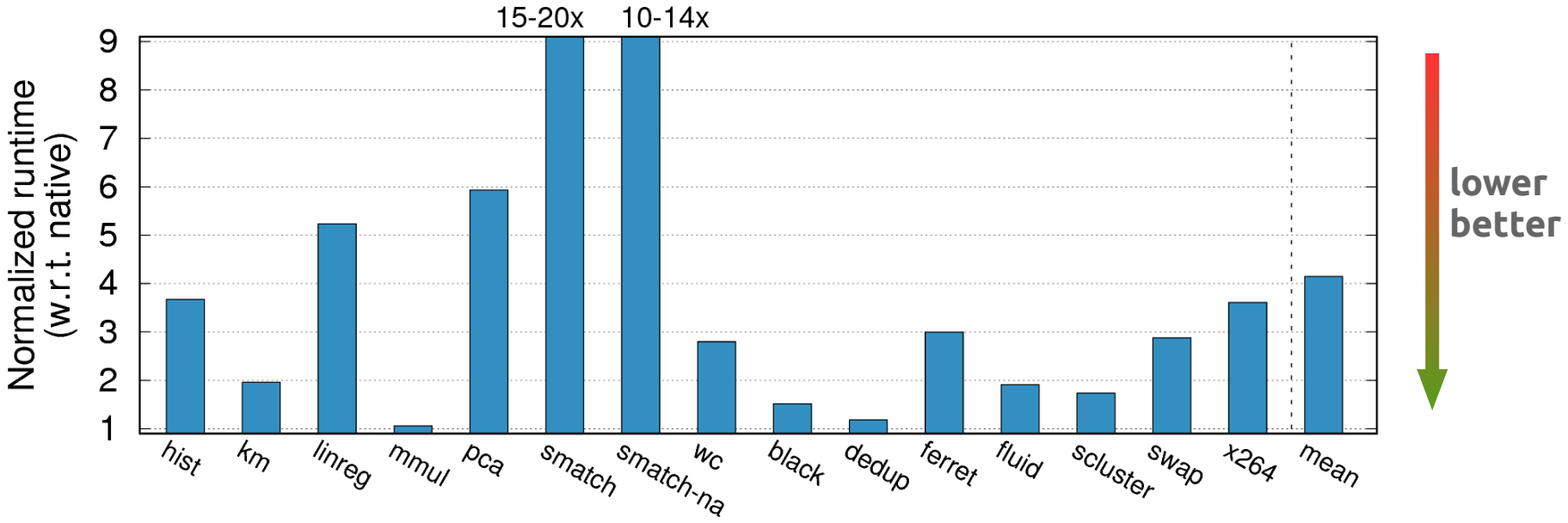
- ☑ Motivation
- ☑ Intel AVX
- ☑ Design
- ☐ **Evaluation**
- ☐ Discussion

Performance overheads

Performance overheads



Performance overheads



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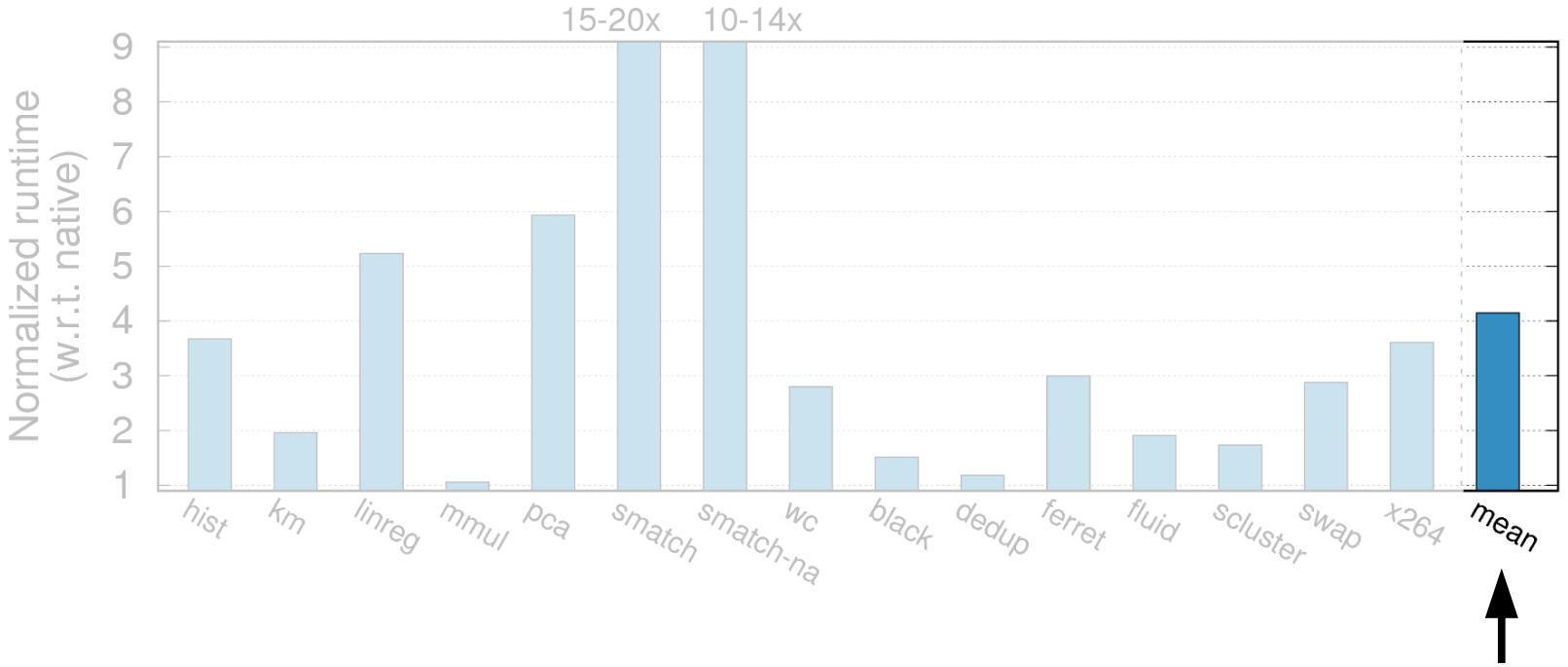
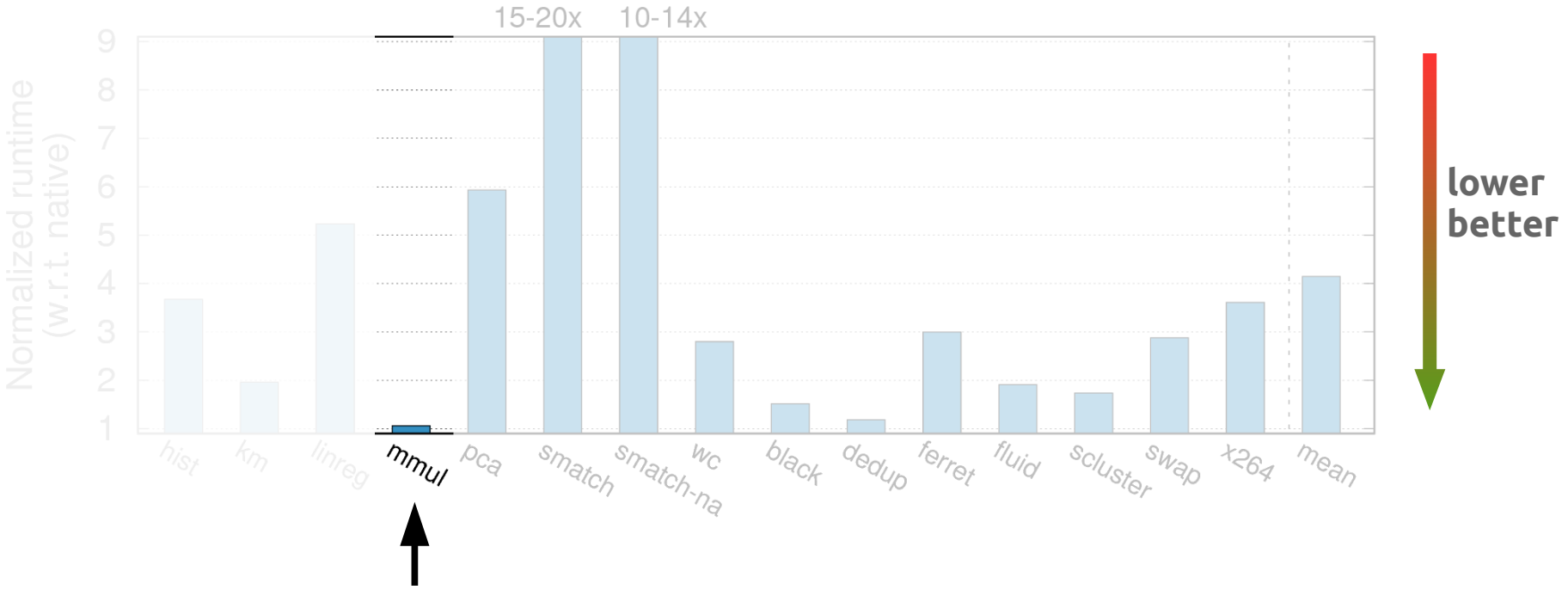


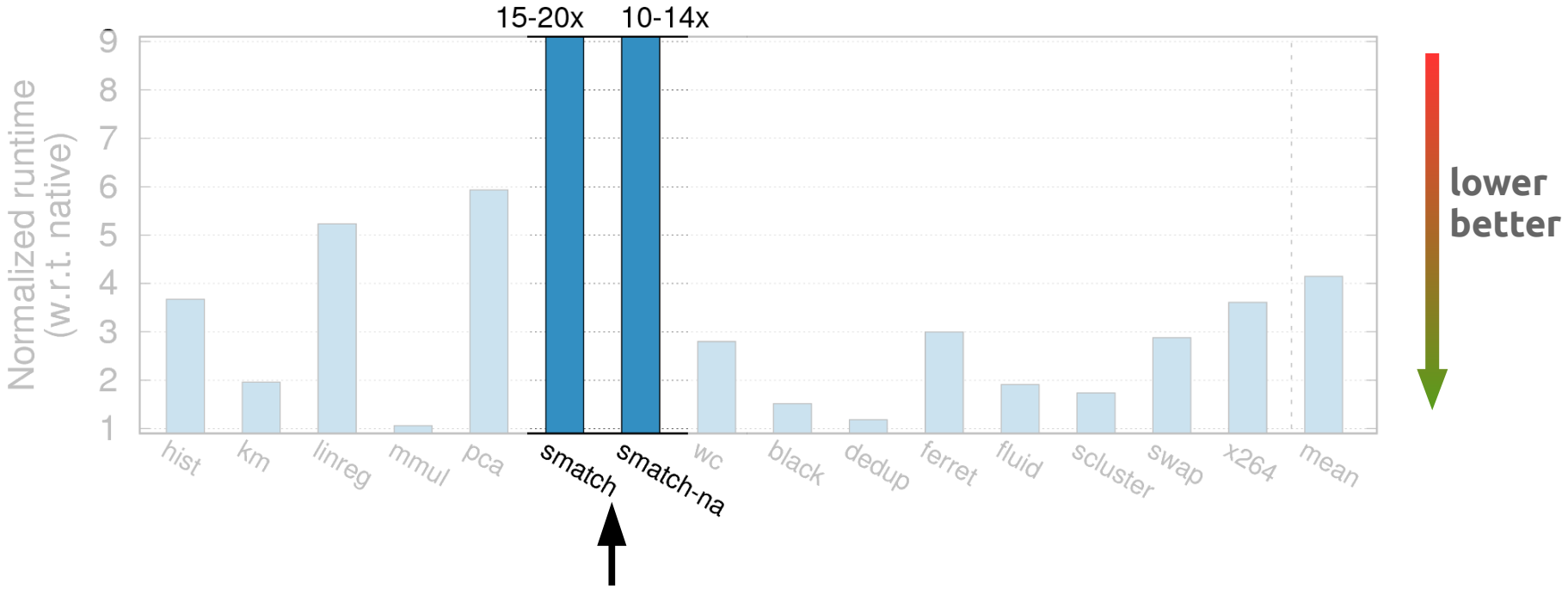
Average performance overhead is **4×**

Performance overheads



Amortized by very poor memory access pattern

Performance overheads



(1) Native benefits from AVX vectorization

(2) Most of time spent in mem-intensive `bzero()`

Comparison with SWIFT-R (state-of-the-art TMR approach)

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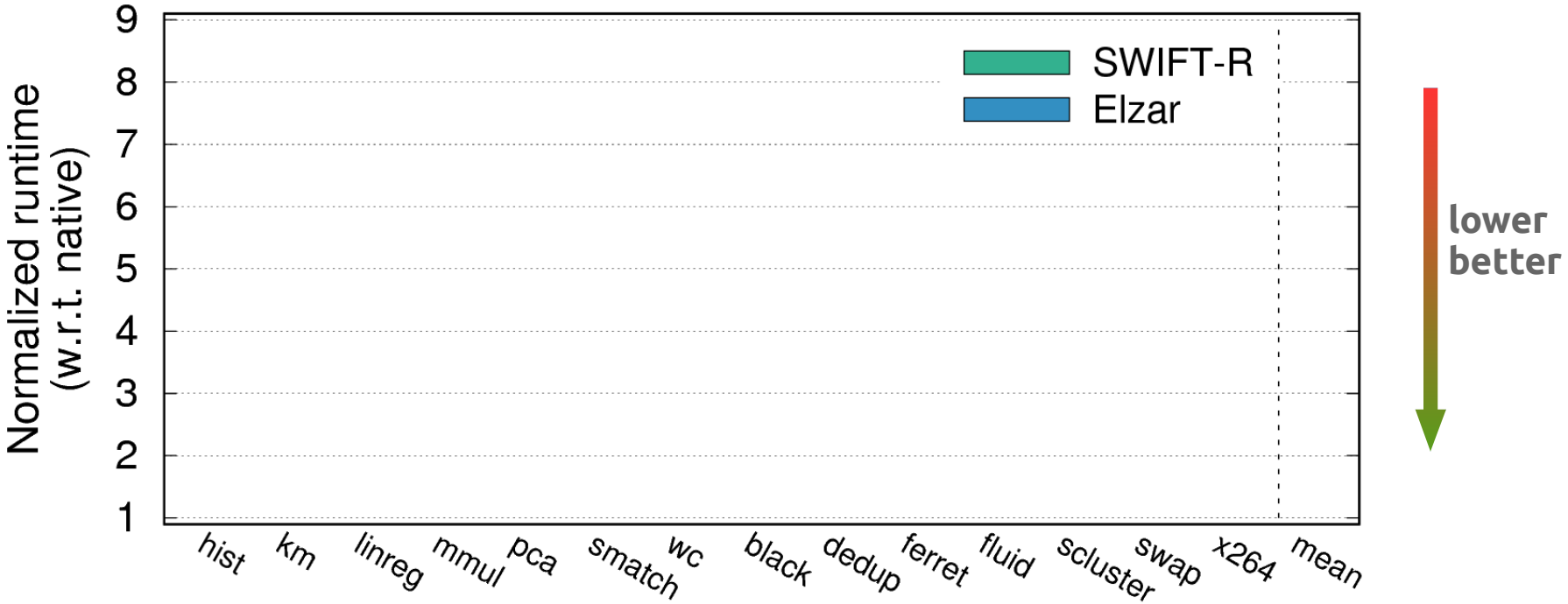

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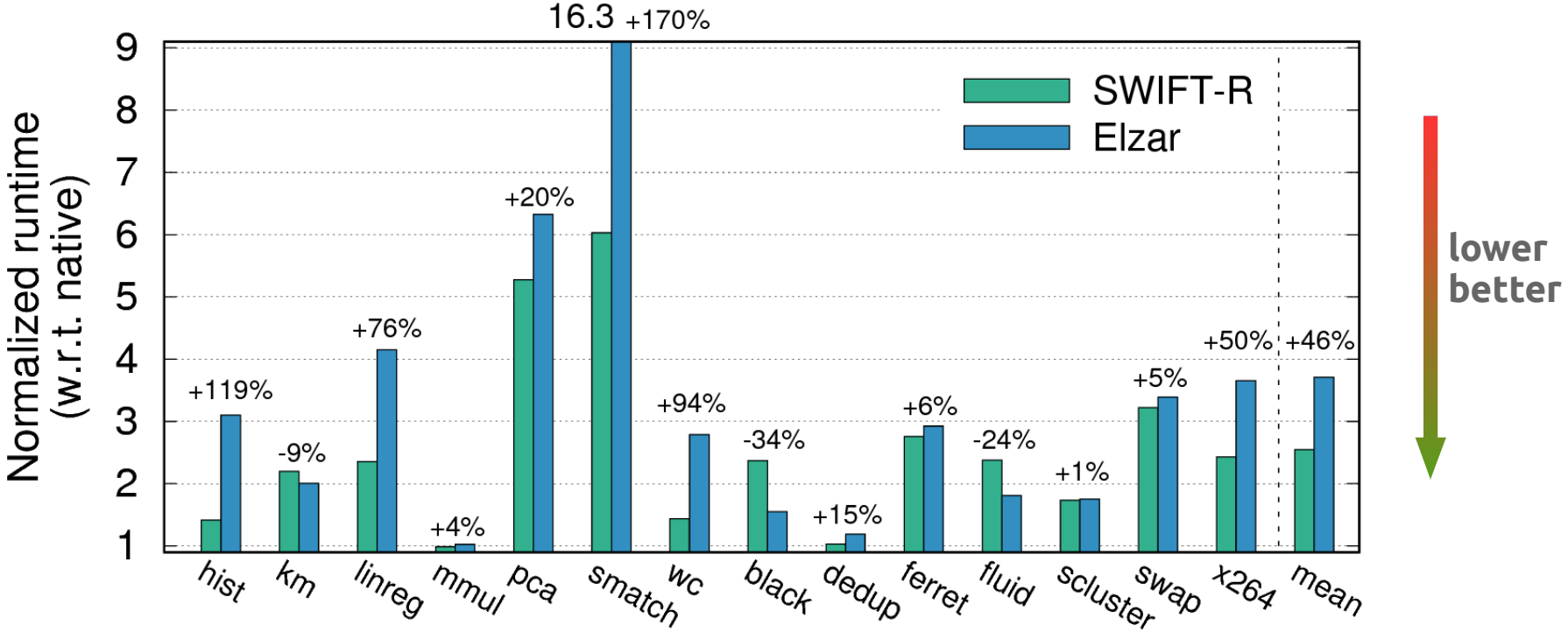

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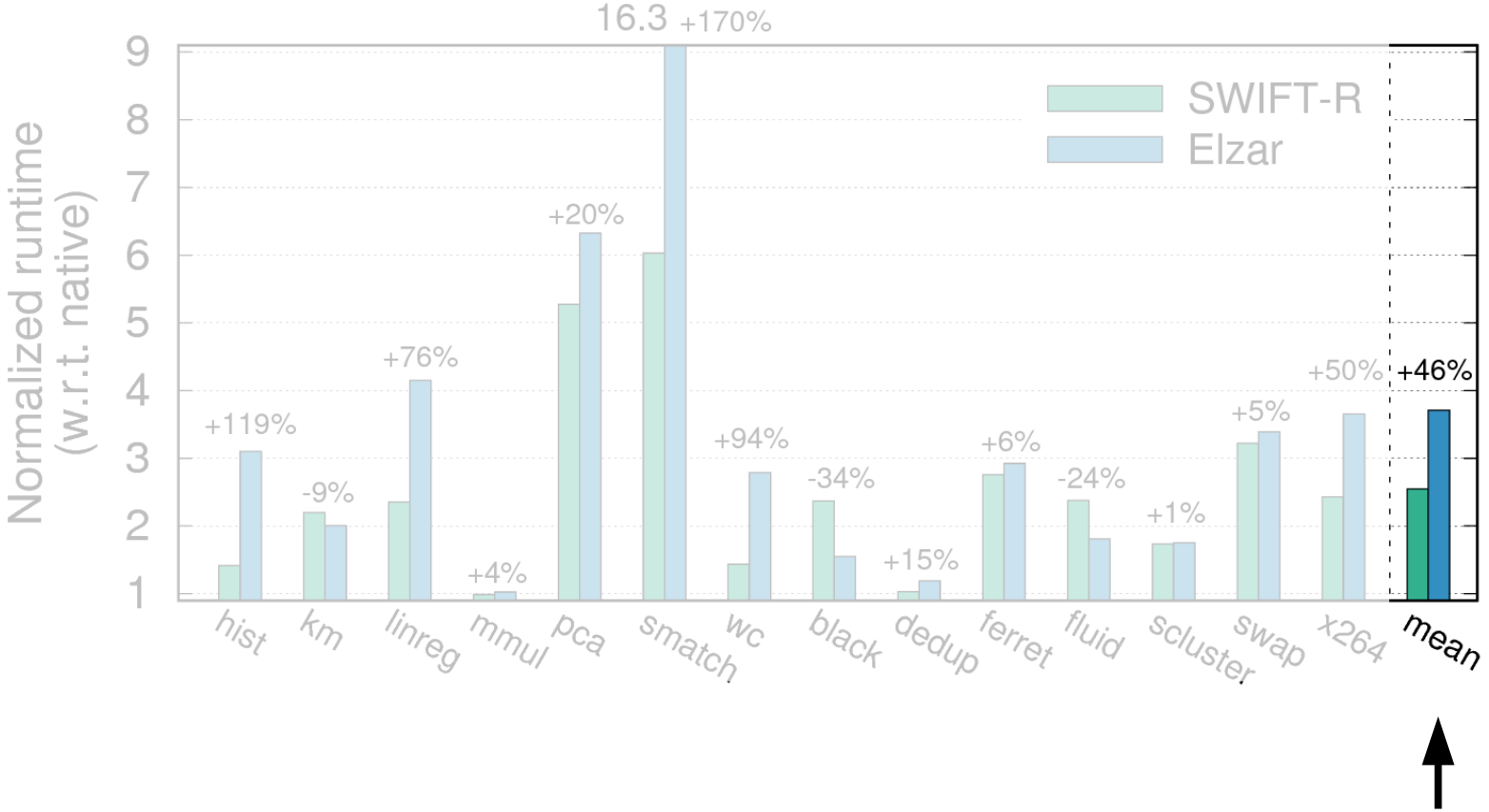
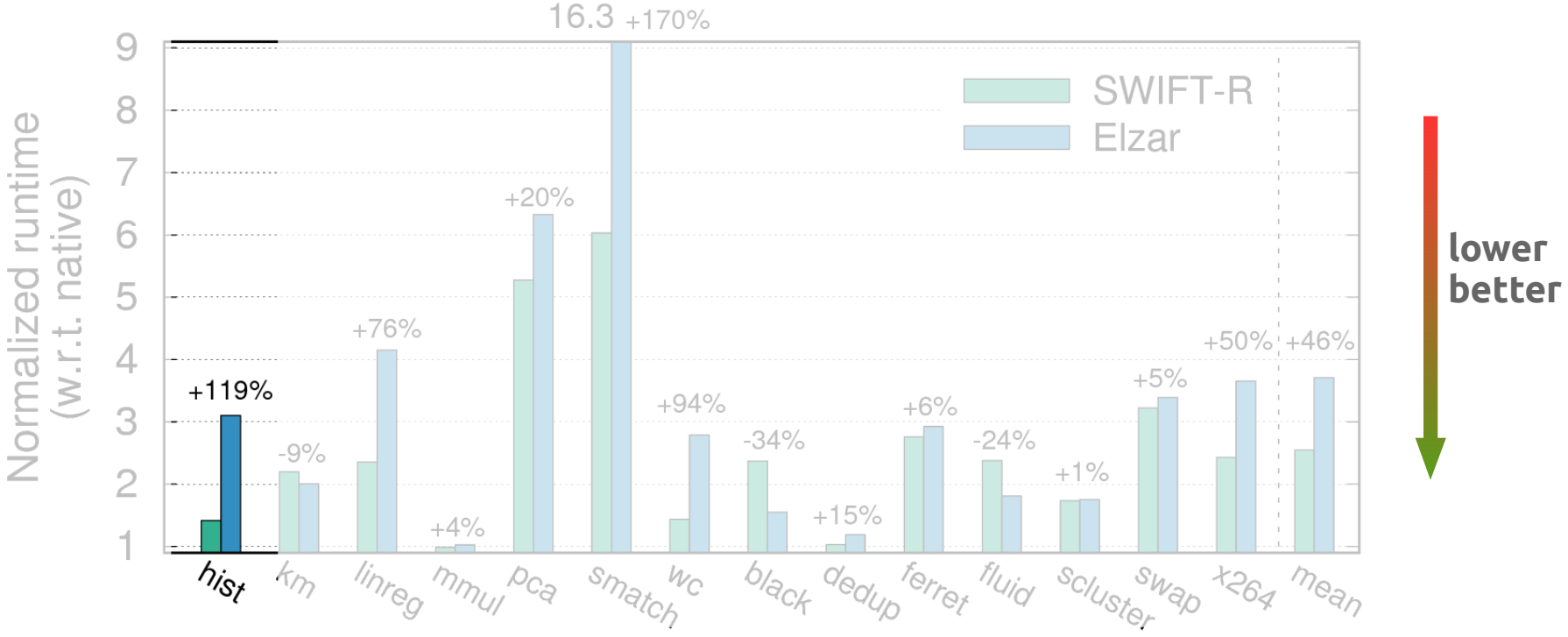


Elzar performs **46%** worse than SWIFT-R on average ☹

Comparison with SWIFT-R (state-of-the-art TMR approach)



Dominated by memory accesses, Elzar inserts many wrappers ☹

Comparison with SWIFT-R (state-of-the-art TMR approach)

Elzar produces **3x less** instructions than SWIFT-R ☺

- ☑ Motivation
- ☑ Intel AVX
- ☑ Design
- ☑ Evaluation
- ☐ **Discussion**

Bottlenecks and Proposed Solution

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AVX lacks certain instructions

- Need wrappers for memory accesses
- Need `shuffle-xor-ptest` for checks

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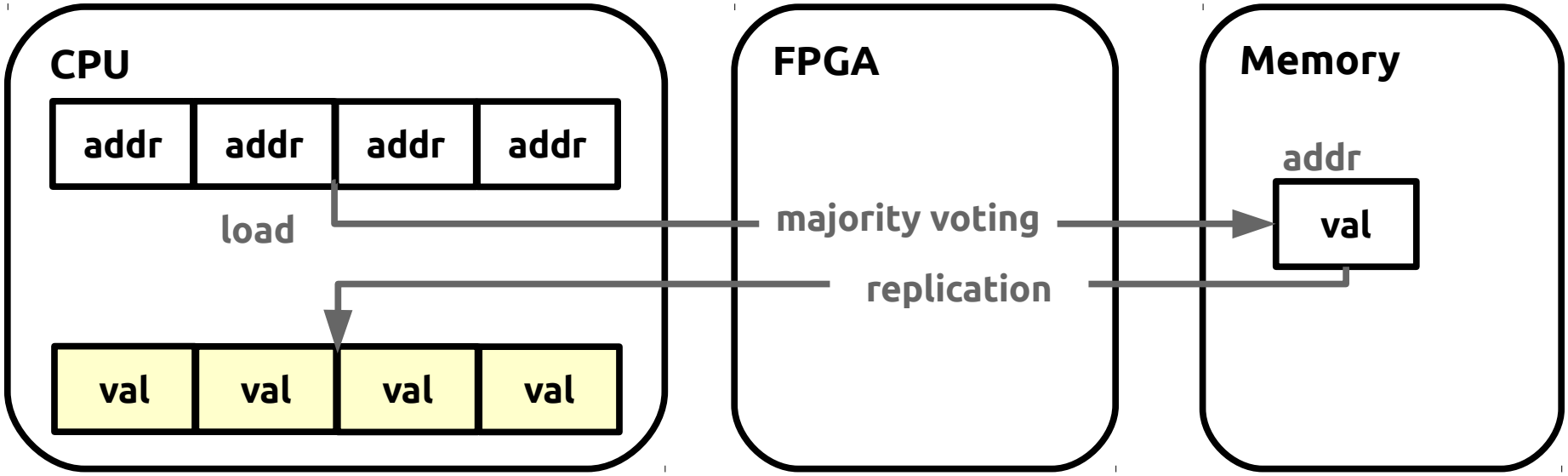

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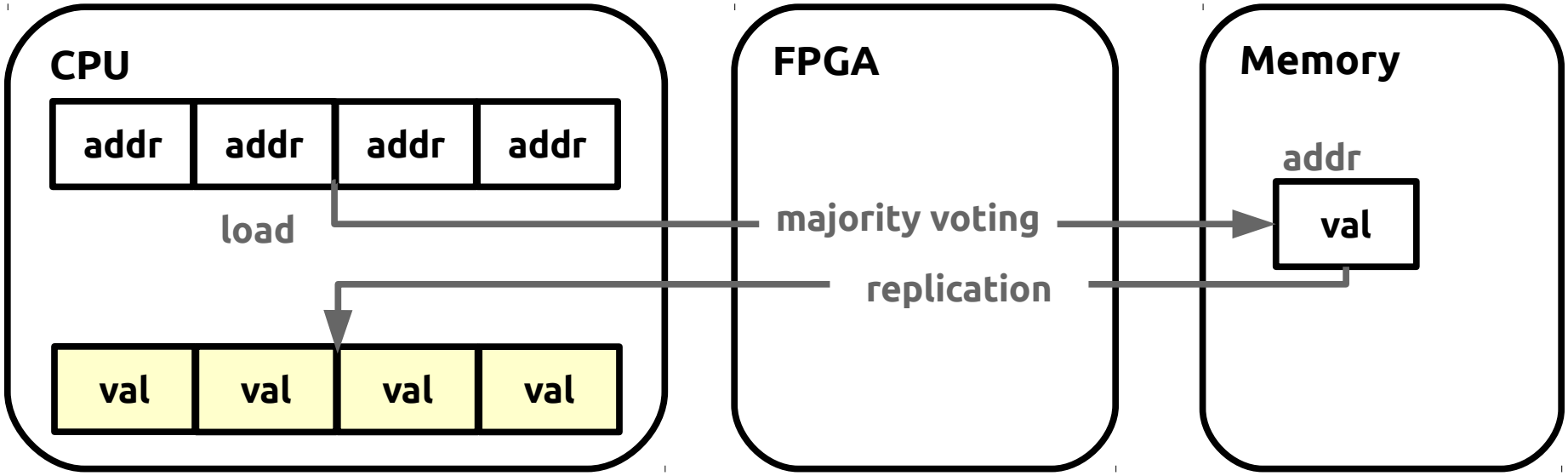

Potentially **71% better** than SWIFT-R

Conclusion

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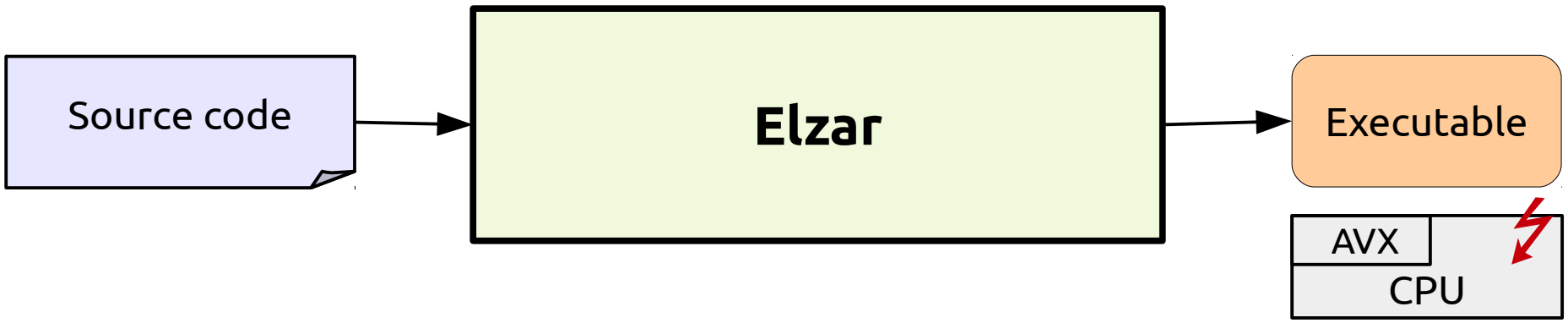

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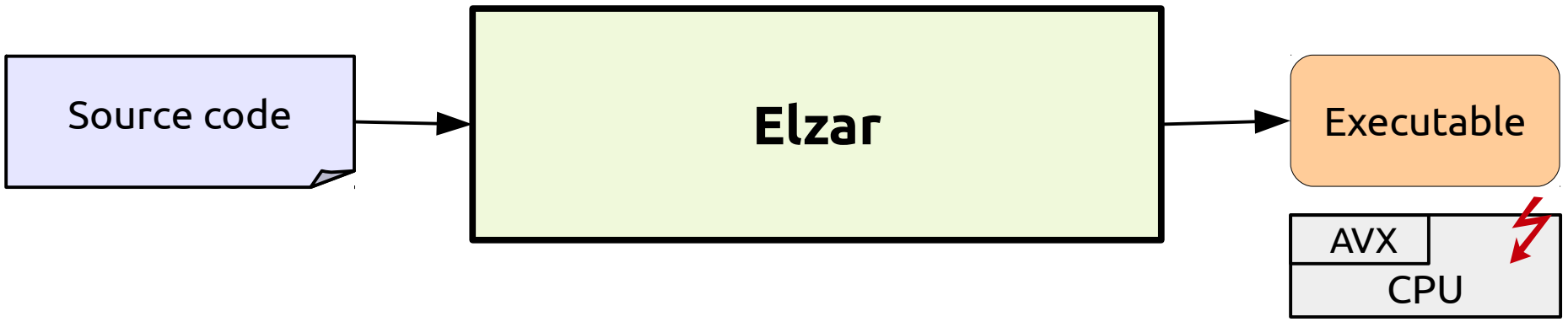
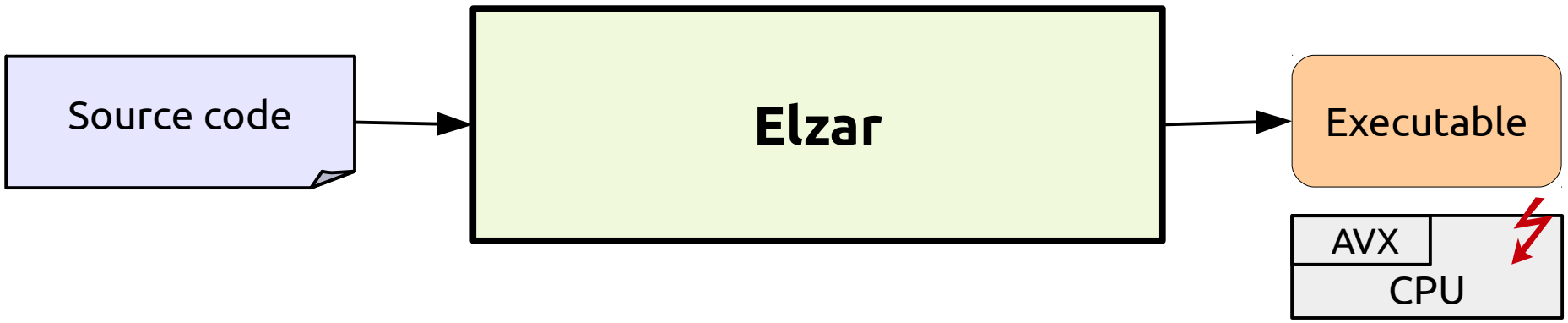


Implementation **Intel AVX** for triple modular redundancy

Conclusion



Implementation **Intel AVX** for triple modular redundancy

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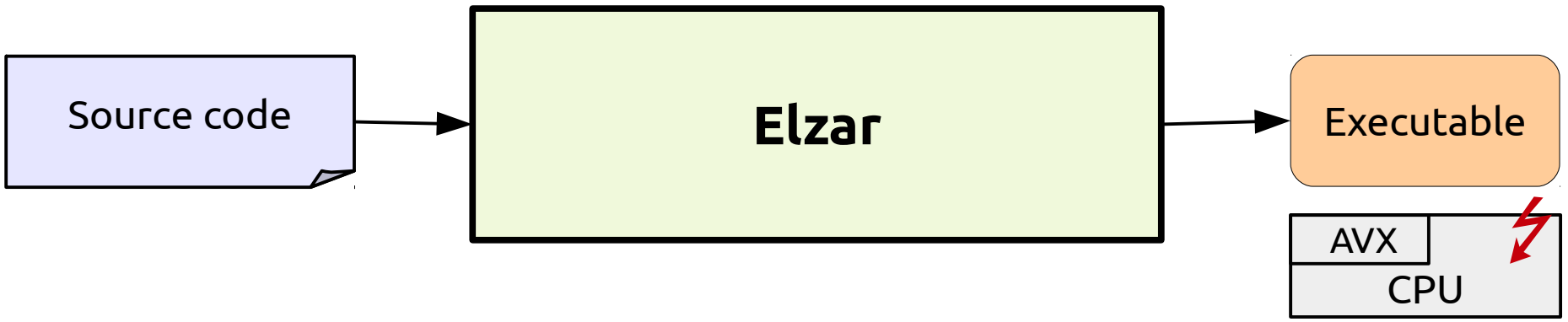

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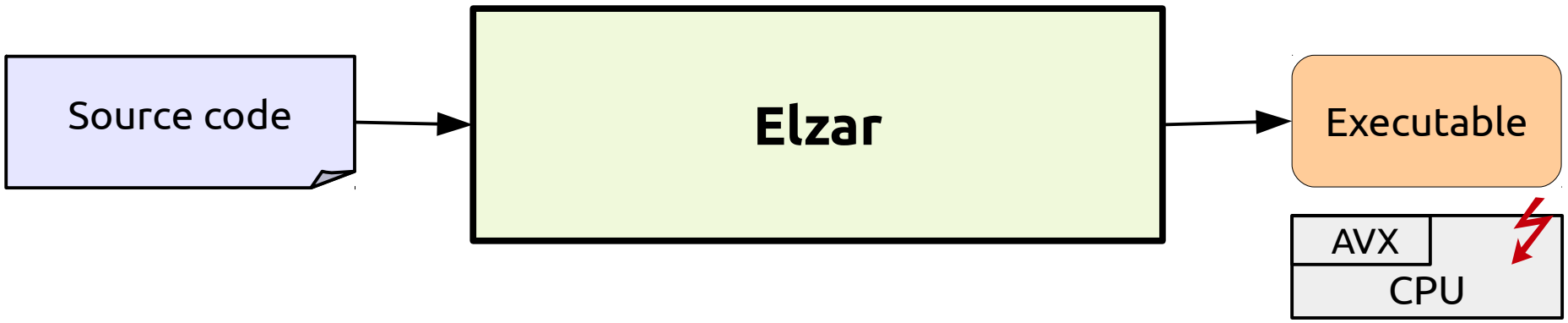


Implementation	**Intel AVX** for triple modular redundancy
Hypothesis	**Less** instructions → **less** perf overhead
Outcome	**46%** worse than SWIFT-R
Discussion	With FPGA, **~71%** better than SWIFT-R

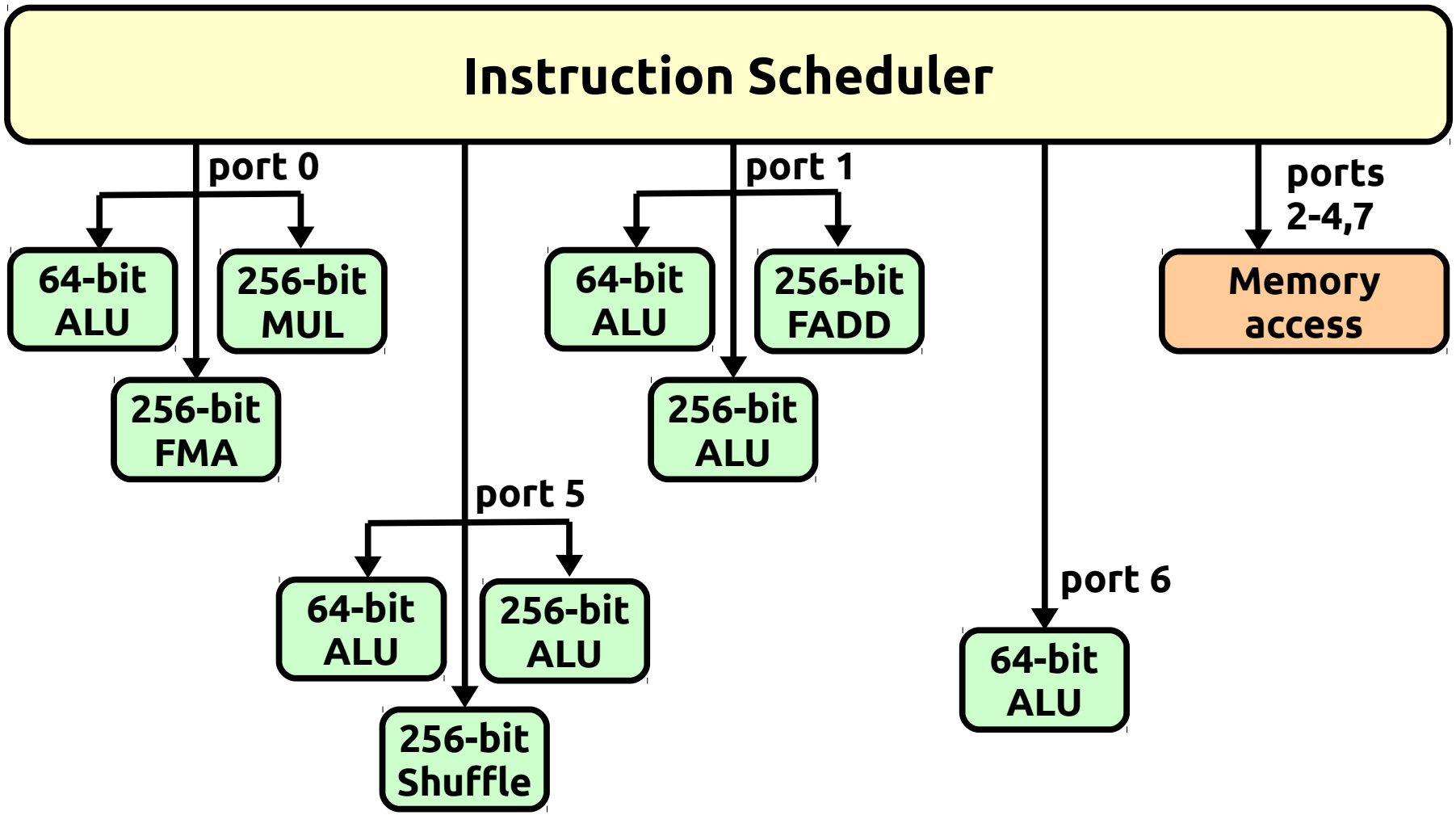
Thank you!

dmitrii.kuvaiskii@tu-dresden.de

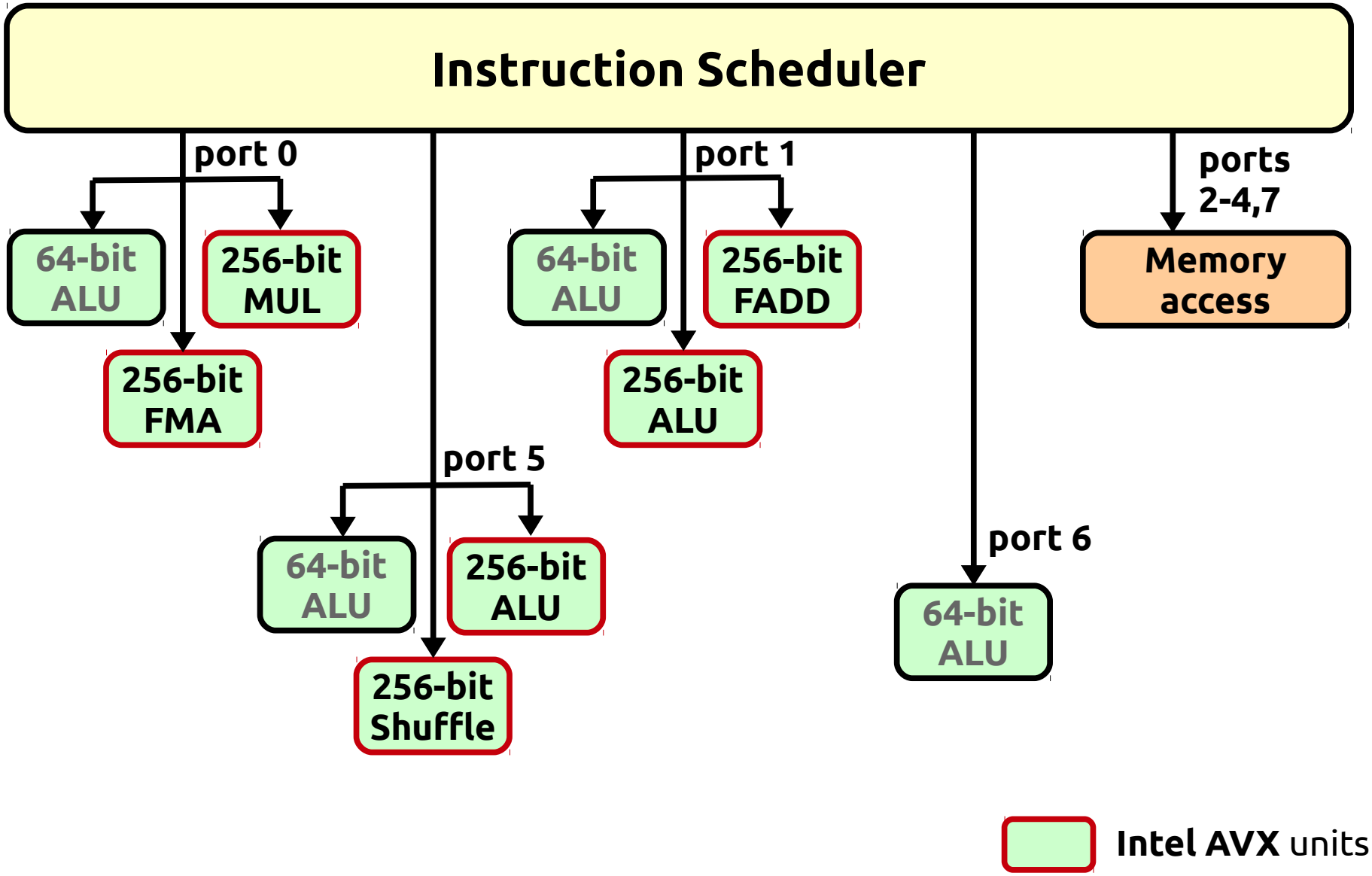
GitHub repo: https://github.com/tudinfse/elzar

backup slides

Intel Haswell CPU microarchitecture



Intel Haswell CPU microarchitecture



Elzar: Check on Branch

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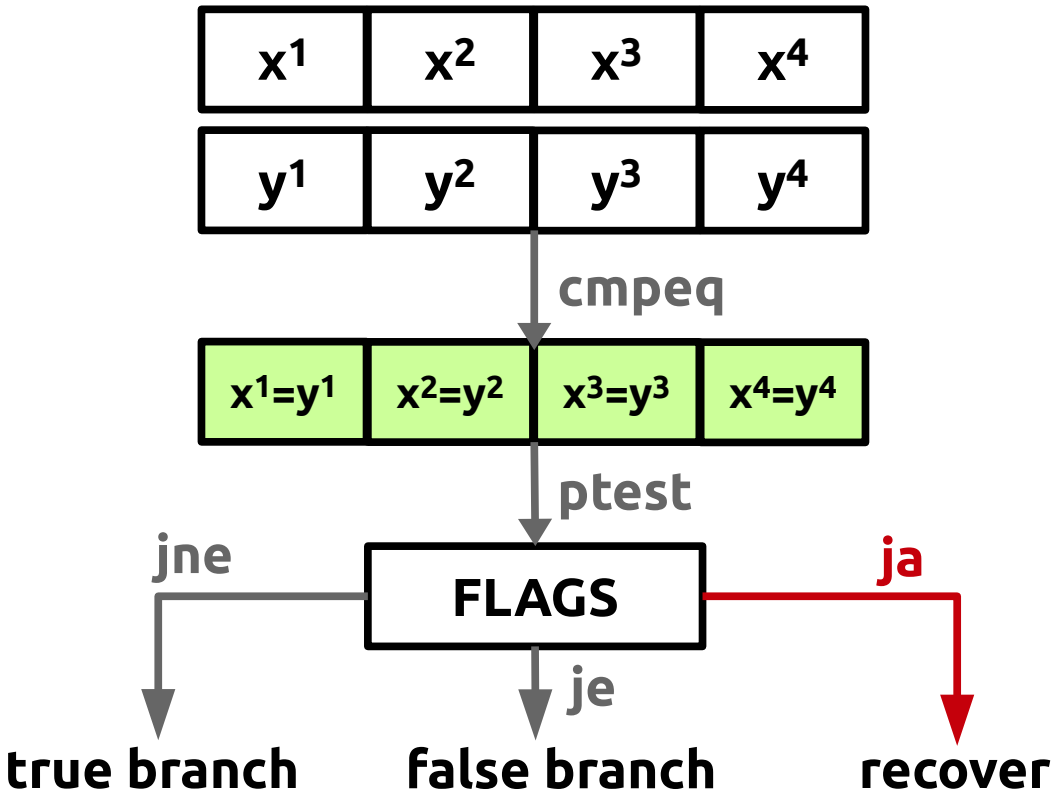

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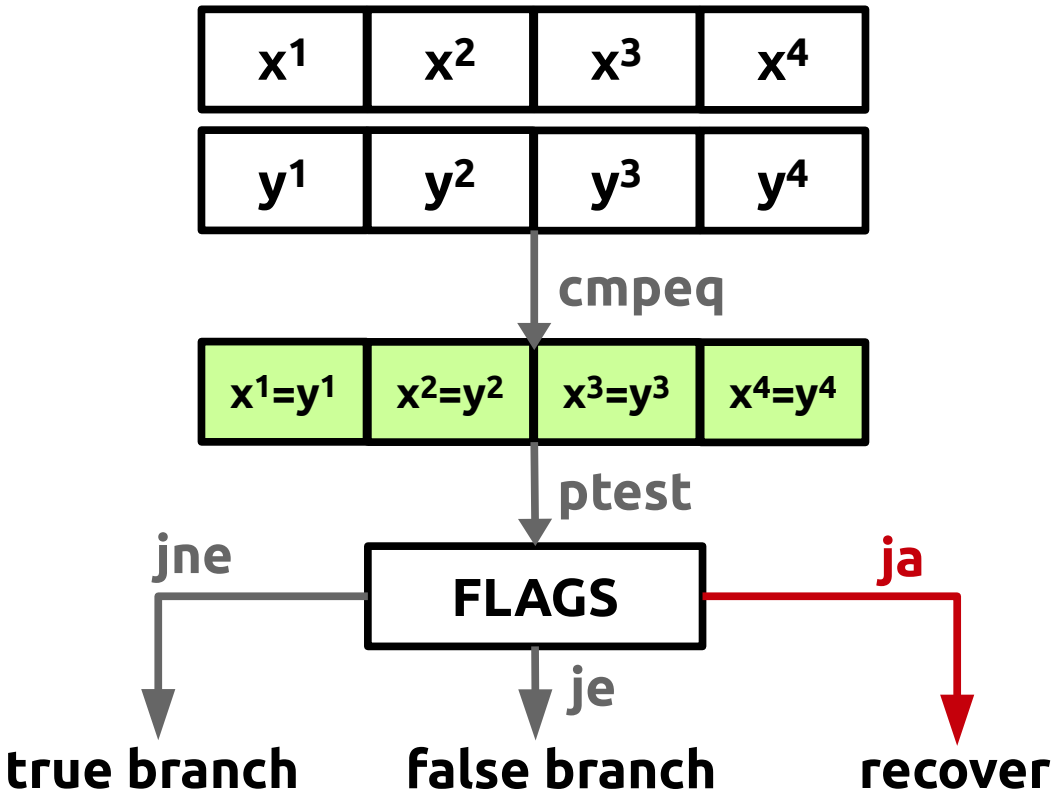


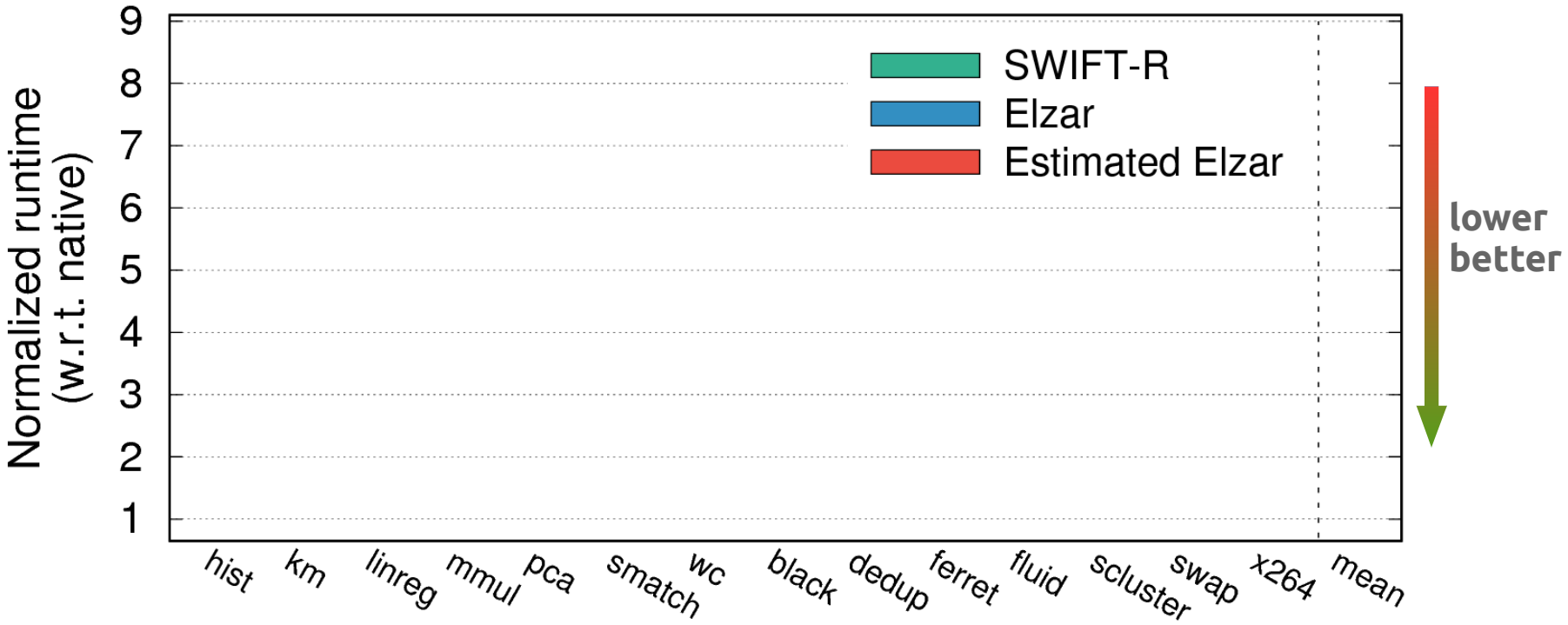
Impact **Checks on branches** introduce only **4%** overhead ☺

Main Bottlenecks

Problem **AVX** instruction set lacks certain instructions

- Loads/stores require extracting AVX-replicated address
  - Elzar creates expensive wrappers around loads/stores
  - AVX-512 introduces promising **`gather/scatter`** instructions
- AVX has only one control-flow instruction `ptest`
  - Elzar has to insert **`ptest`** for each control-flow decision
  - AVX could add **`cmp`** instructions directly affecting control flow
- AVX misses integer division, integer truncation, etc…
  - Elzar produces very ineffective code in these cases

Estimation of Proposed Changes



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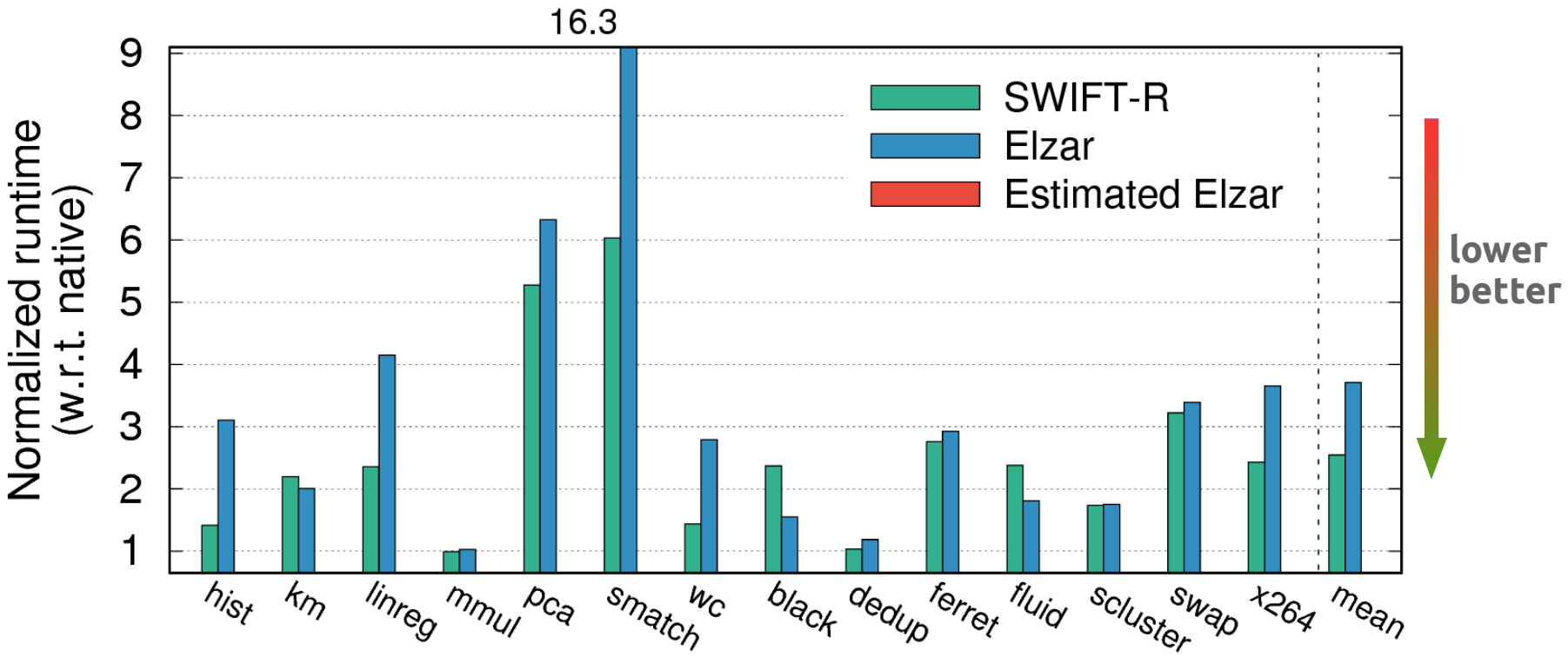

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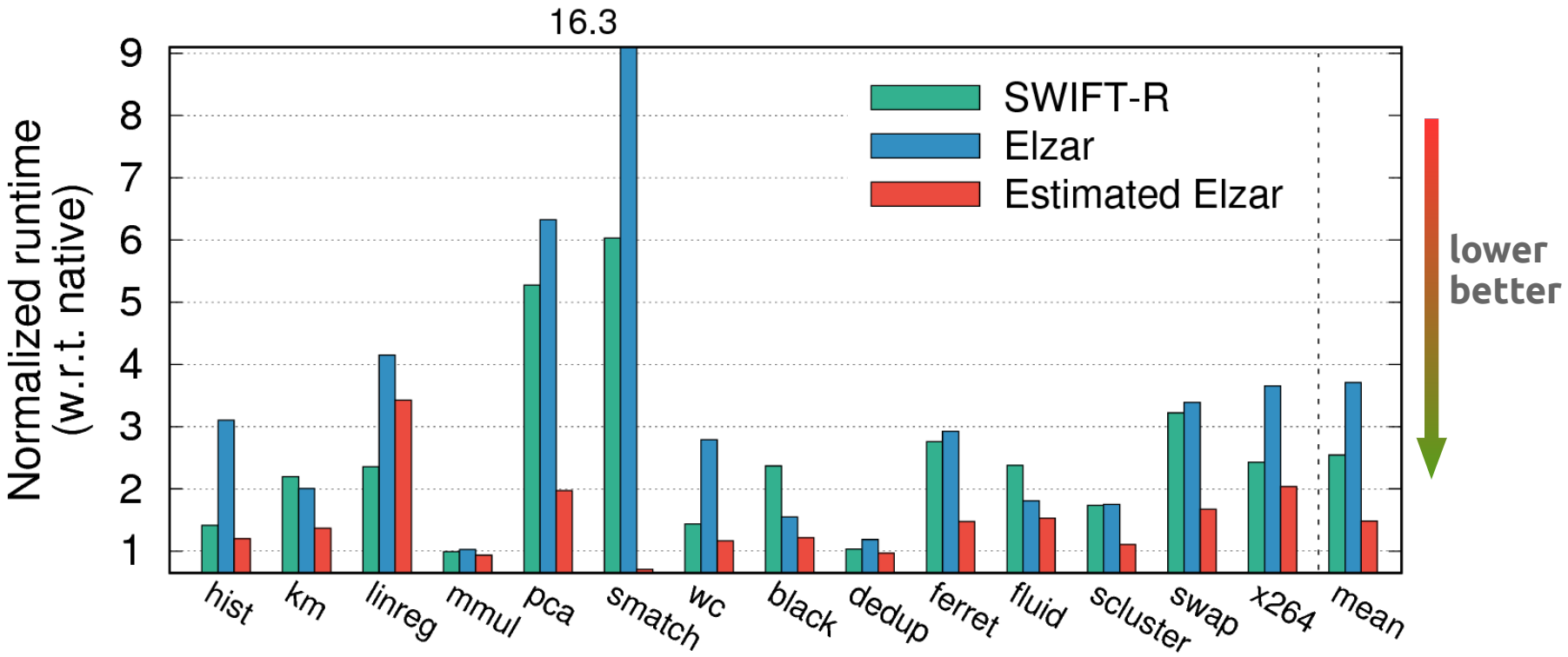

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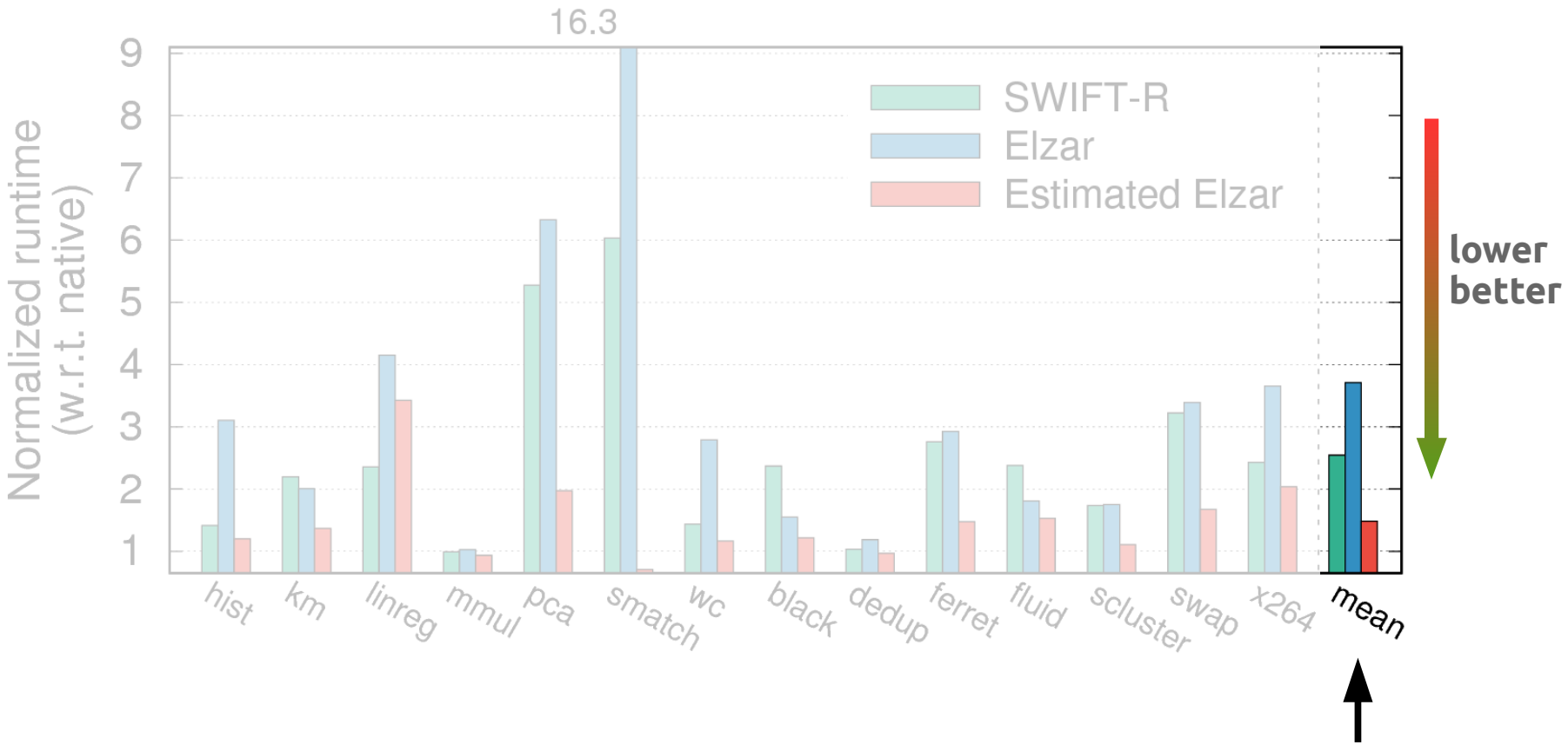

Estimated average overhead would be **48%**
(**71%** improvement over SWIFT-R)